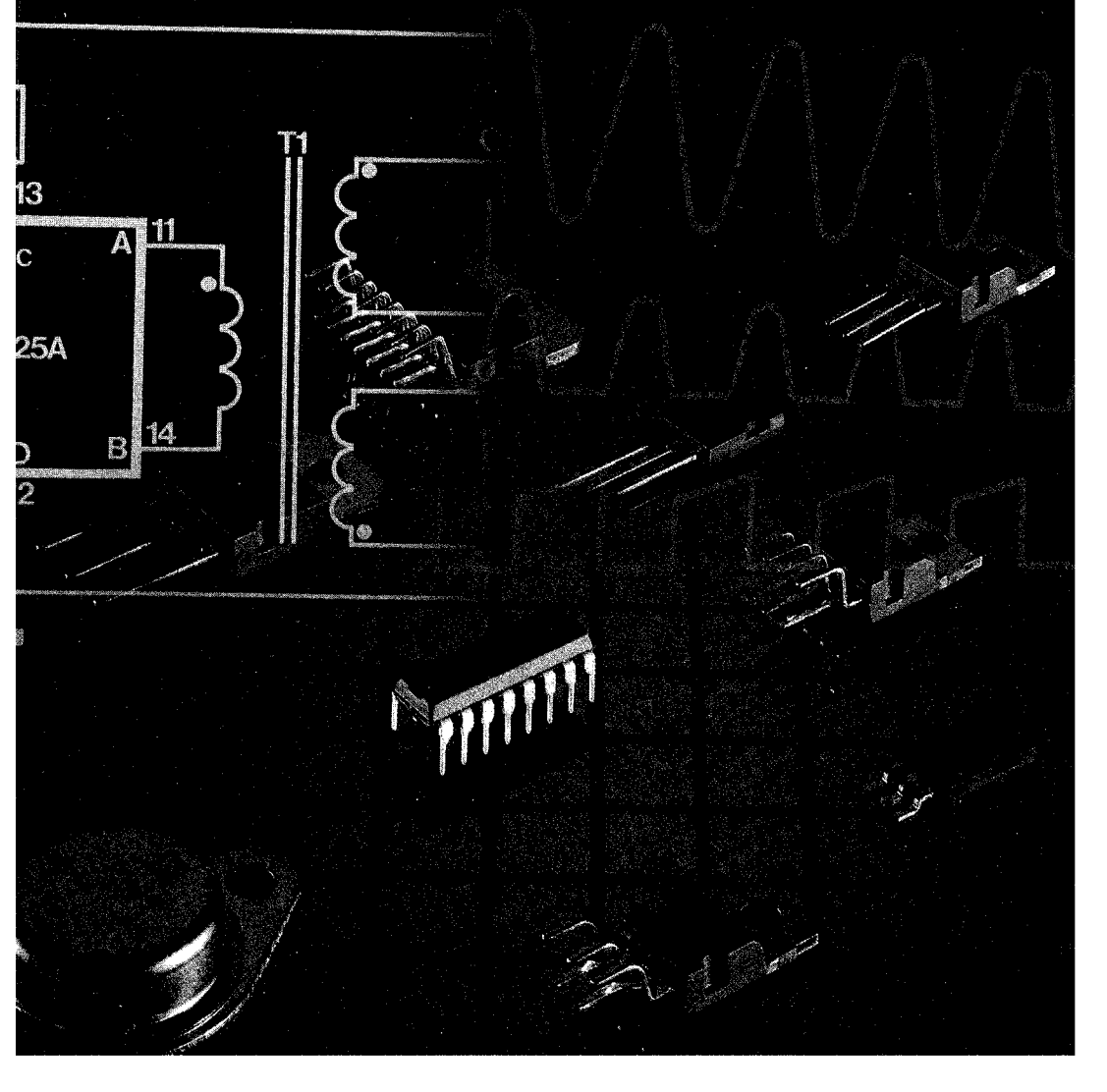
SGS®

Technology and Service

POWER SUPPLY APPLICATION MANUAL



Power Supply Application Manual

July 1985

IDENTITY

Late in 1957, SGS was founded around a team of researchers who were already carrying out pioneer work in the field of semiconductors. From that small nucleus, the company has evolved into a Group of Companies, operating on a worldwide basis as a broad range semiconductor producer, with billings well over a quarter billion dollars and employing over 10000 people.

The SGS Group of Companies has now reached a total of 11 subsidiaries, located in Brazil, France, Germany, Italy, Malta, Malaysia, Singapore, Sweden, Switzerland, United Kingdom and the USA.

To go with its logo, the company takes the motto "Technology and Service", underlining the accent given to the development of state-of-the-art technologies and the corporate commitment to offer customers the best quality and service in the industry.

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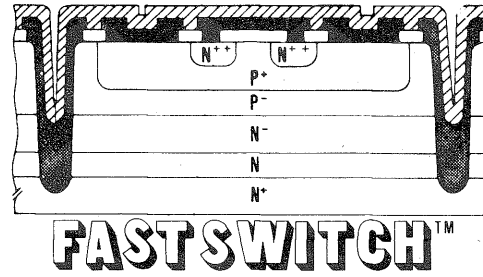
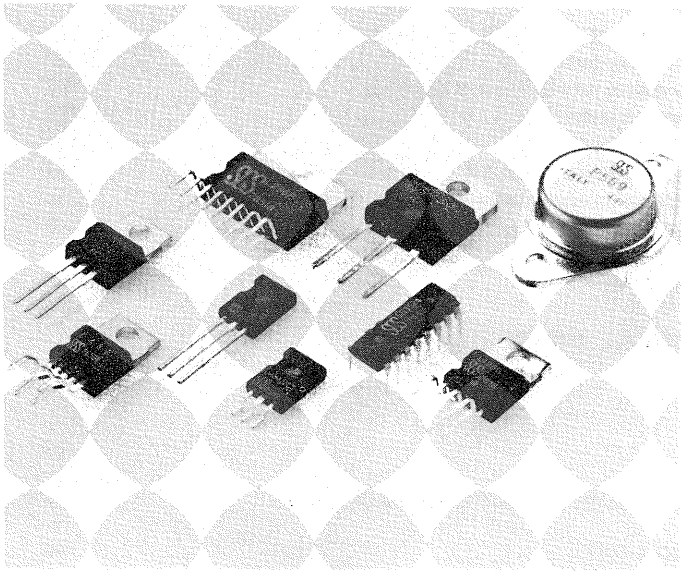
THE NUMBER ONE SOURCE FOR POWER SUPPLY SEMICONDUCTORS

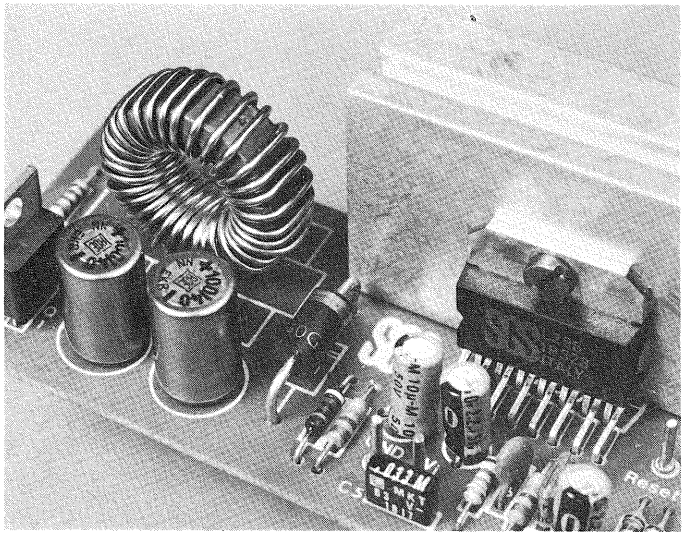
Thanks to a long tradition of innovation in power IC and transistor technology, SGS offers the industry's most complete range of products for power supply applications.

Highlights of this product range include unique technological leadership products such as the L296 High Power Switching Regulator family and the FASTSWITCH™ range of ultrafast high voltage transistors.





SGS offers the industry's most complete range of semiconductors for power supply applications.



The SGS range includes world-beating products like the L296, a switching regulator IC that delivers 4A at 5V to 40V.

SGS also produces innovative voltage regulator ICs with features such as very low input/output drop, microprocessor reset functions and rugged protection circuitry for automotive applications. And the power transistor range of more than 1000 devices includes more than 300 POWER MOS types plus devices in a new isolated plastic package similar to the SOT-93/TO-218. In 1985 SGS will also introduce a family of fast recovery epitaxial diodes covering 2A to 40A and 50V.

The same expertise in design and production is also applied to produce a wide range of standard devices in high volumes with exceptionally competitive quality and service. The formidable production resources of SGS bring not only high volume capability, but also the security of internal second sourcing, with four separate 5" wafer front ends for linear ICs and three separate diffusione facilities, two of them 5", for power transistors.

These world-beating wafer fabs are followed by modern assembly facilites using the highest level of automation available.

SGS now applies its power semiconductor technology to produce a range of DC-DC converter modules, the GSR-400 family. Available with a wide range of input voltages, these compact modules include supply features such as microprocessor reset, crowbar protection, remote on/off control and current limiting.

Backing up this impressive product range is a worldwide network of SGS sales offices and distrinutors. In addition, SGS' local design centers in the USA, England, France, West Germany, Italy and Singapore simplify the development of new products to satisfy the special needs of your applications.

New diffusion facilities give SGS the advantage in Service, Quality and cost. State-of-the-art 5" wafer fabs are used for both linear ICs and power transistors.

POWER SUPPLY APPLICATIONS

50W OFF LINE SWITCHING POWER SUPPLY USING THE UC3840

INTRODUCTION

This power supply has been designed to provide an easy way to gain familiarity with the operating characteristics of the UC3840 PWM Control Circuit in a pratical off-line power supply application. As any switching power supply represents a series of compromises between size, cost, efficiency, performance, and many other variables; no claim is made that this supply optimizes any particular characteristics; only that it provides an easy means to gain an understanding which, hopefully, the designer can use to extrapolate to many specific applications.

This power supply, shown schematically in Fig. 4 implements a 50 watt discontinuous mode flyback power supply with multiple outputs, and features primary-side control with full protection from fault conditions. Additional performance characteristics include simple off-line starting, voltage feed-forward for good line regulation (without feedback across the isolation boundary), pulse-by-pulse current limiting, over- and under-voltage sensing with protective shutdown and automatic restart, and freedom from the need for any circuit adjustments.

For additional information on the operation of the UC3840, reference should be made to TN 168 and data sheet.

POWER SUPPLY SPECIFICATIONS

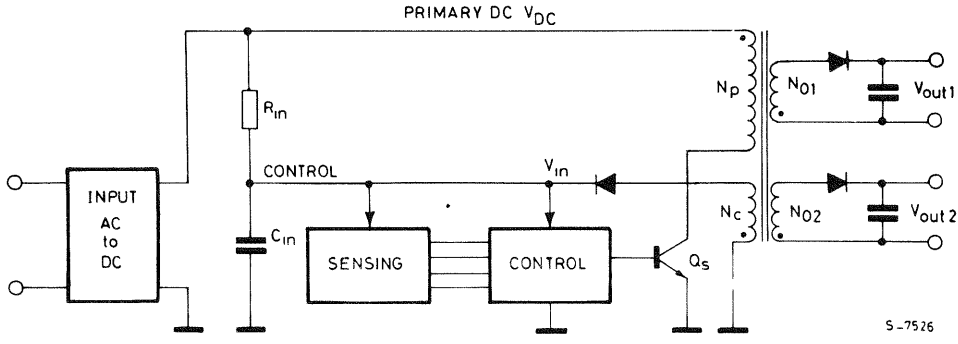
Input line voltage:	
With 110V jumper:	90 VAC to 130 VAC
With jumper removed:	180 VAC to 260 VAC
Input frequency:	50 or 60 Hz
Switching frequency:	40KHz ± 10%
Output power:	50W maximum
Output voltages:	5V ± 5% 12V ± 5%
Output current:	2.5 to 5A (5V) 1 to 2A (12V)
Line regulation:	5V, 0.07% /V 12V, 0.04% /V
Load regulation:	5V, 2.5%/A 12V, 2.5%/A
Efficiency @ 50 watts	
V_{in} = 90 VAC:	70%
V_{in} = 130 VAC:	65%
Output ripple:	5V @ 5A = 200mV 12V @ 2A = 300mV

OPERATING PRINCIPLES

In an off-line switching power supply, the input voltage is immediately rectified and filtered, and the resulting DC voltage is chopped at a high frequency. Where 110/220 VAC operation is required, an input voltage doubler configuration is used for 110 VAC input, resulting in a nominal DC input voltage of 310V. The same nominal input voltage is obtained with full wave rectification of a 220 VAC line input. High frequency switching allows a very small transformer to be used to efficiently step down to lower output voltages. In the configuration shown in Figure 1 an additional low-voltage winding, N_c, is used to provide continuous operating power for the control and base drive circuits. However, initial energy to start the supply is taken from the line via R_{in} and C_{in}. An additional function on N_c is to provide a primary-referenced feedback voltage that is proportional to the output voltages. This feedback voltage is sensed and regulated by the control circuitry, thereby eliminating the need for feedback across the isolated boundary.

The polarity of the transformer windings identifies this configuration as a flyback supply. When transistor Q_s conducts, all output diodes are reverse biased and the energy is stored in the primary inductance. When Q_s turns off, the voltage polarity of winding N_p reverses (flies back) and the energy is delivered to the output circuits. This circuit operates in the discontinuous mode in which all the energy stored in the trasformer inductance is completely transferred to the load during every cycle, i.e. transformer current goes to zero before the end of each cycle. Although this approach yields higher peak current compared to other topologies, it is usually chosen because of its less stringent requirements on the transformer, its faster transient response, and its easier stabilization. To insure discontinuous operation and core reset, the volt-second product across the transformer primary during reset must be allowed to equal or exceed the volt-seconds applied during the on-time of Q_s.

Fig. 1 — Simplified block diagram of a flyback power supply with primary control



DESIGN CONSIDERATIONS

The following description of the design decisions made for this power supply will be with respect to the complete schematic shown in Fig. 4. No significant theoretical discussion is offered and only nominal values are used in the analysis, but hopefully the equations given can be used to either extrapolate to other design problems or to optimize the supply to a particular characteristics.

Input section

Input bridge D1 rectifies the line voltage while resistors R1 and R2 are used to limit the peak charging current to capacitors C1 and C2. The values for C1 and C2 are usually determined by either the ripple voltage allowable for V_{DC} or the minimum hold-up time.
Ripple calculations are worse-case for the 110V voltage doubler configuration where:

RMS line voltage = 90 to 130 VAC
peak no-load input = 253 to 368 volts.

At the minimum line voltage, each capacitor alternately charges to a peak of 126 volts. Allowing for a total input voltage sag at full load of 50 volts, the minimum capacitor voltage must be held to 92 volts. Since each capacitor must provide one-half the energy requirements of the power supply, the required energy for each line cycle is:

$$W_{in} = \frac{\text{Power out}}{\text{Efficiency x Frequency}} = \frac{50}{0.7 \times 60} = 1.2 \text{ Joule}$$

and the capacitor value can be calculated from:

$$\tfrac{1}{2} W_{in} = \tfrac{1}{2} C_1 \quad (V_{pk}^2 - V_{min}^2) \text{ or}$$

$$C_1 = \frac{W_{in}}{V_{pk}^2 - V_{min}^2} = \frac{1.2}{126^2 - 92^2} = 162\mu F$$

If, instead of ripple voltage, we choose the input capacitors to hold the input DC above 200 volts for a least two cycles of line drop-out, then:

$$C_1 = \frac{2\,(Po/2)\,(\text{no. of cycles drop-out})\,1/f}{\text{Efficiency}\,(V_{pk}^2 - V_{min}^2)}$$

$$= \frac{2\,(25)\,(2)\,1/60}{0.7\,(126^2 - 92^2)} = 331\mu F$$

In this application, 470μF was picked as a standard size which would allow loose tolerances.

Transformer

A major task with any flyback power supply is the design of the transformer as many tradeoffs are normally required between regulation, leakage inductance (and corresponding transistor stress), isolation, size, and cost. In this application, the core selected is a Ferrox-cube EC35-3C8 which has the following characteristics:

Effective core area, $A_e = 0.84$ cm^2
Max flux density, $B_{sat} = 2800$ gauss
Bobbin = 35 PC B I

The design starts with a calculation of maximum duty cycle which is defined by the voltage capability of the power switch. This voltage was allocated as follows:

VDC max	= 370V
Reset voltage	= 120V
Leakage inductance spike	= 100V
Max total voltage	= 590V

With a reset voltage of 120V, at minimum input voltage,

$$D_{max} = \frac{120V}{120V + 200V} = 37.5\%$$

The primary inductance can then be calculated as:

$$L_p = \frac{\text{Efficiency}}{2\,P_o\,f}(V_{in\,min} \times D_{max})^2 =$$

$$= \frac{0.7\,(200 \times 0.375)^2}{2 \times 50 \times 40 \times 10^3}$$

$$L_p \approx 1\text{mh}$$

The peak current at full load is:

$$I_p = \frac{2P_o}{\text{eff}\,(V_{in\,min} \times D_{max})} =$$

$$= \frac{2 \times 50}{0.7 \times 200 \times 0.375} = 1.9A$$

The maximum energy storage requirement within the primary is calculated on the basis of maximum current, in this case assumed to be short circuit current = 120% x I_p or 2.3A.

$$W = \tfrac{1}{2} L\, I_{sc}^2 = \tfrac{1}{2}(1 \times 10^{-3})\,(2.3)^2 = 2.65 \text{ m Joule}$$

The equation defining energy storage in an inductor is:

$$W = \tfrac{1}{2}\frac{BA_cH\ell_e \times 10^{-8}}{0.4\pi} \text{ Joules}$$

Therefore,

$$H\ell_e = (0.4\pi)\frac{2W \times 10^8}{BA_c} =$$

$$= \frac{0.4\pi \times 2 \times 2.65 \times 10^{-3} \times 10^8}{2800 \times 0.84} = 282 \text{ Gilberts}$$

Since $H\ell_e = 0.4\pi NI$, on the basis of $I_{sc} = 2.3A$,

$$N_p = \frac{H\ell_e}{0.4\pi\ I_{sc}} = \frac{282}{0.4\pi \times 2.3} = 98 \text{ turns}$$

The air gap for the core is determined by knowing that

$$H = \frac{B}{\mu} = 2800 \text{ Oersteads}$$

And assuming that with an air gap

$I_e \approx I_g$. , then

$$I_g = 0.4\pi\frac{NI}{H} = \frac{0.4\pi\ (98)\ 2.3}{2800} = 0.1 \text{ cm}$$

With the primary turns defined, each secondary can be calculated from:

$$N_s = \frac{N_p\ (V_o + \text{rectifier } V_f)\ (1 - D_{max})}{V_{in\ (min)}\ D_{max}}$$

With minor adjustments to give an integral number of turns, the final transformer winding specifications are:

First winding — primary — 97 turns, AWG 24
Second winding — 5 volt — 4 turns, 4 parallel AWG 22
Third winding — 12 volt— 9 turns, 2 parallel AWG 22
Last winding — control — 9 turns, AWG 24 evenly spaced along the full bobbin length

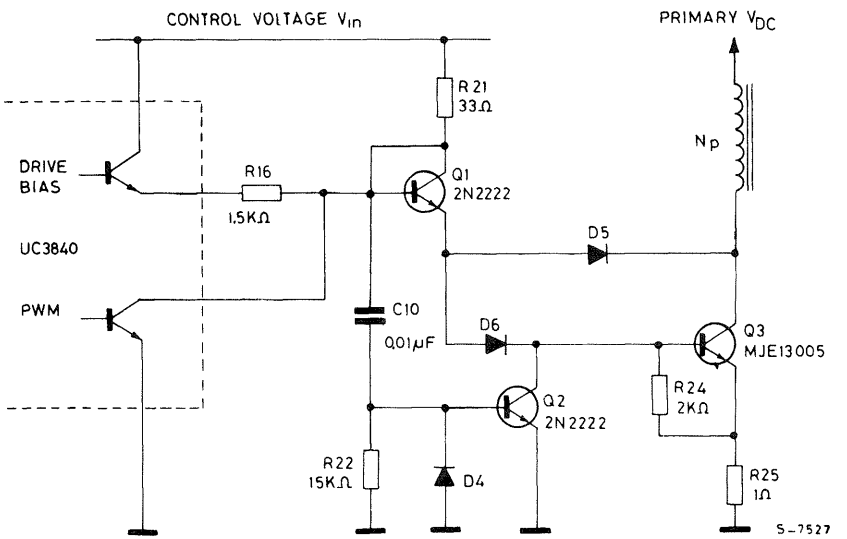
Power switch and drivers

In this application, the peak switch current is 2.3 amps and the peak collector voltage will be approximately 590 volts including the spike caused by leakage inductance. The switching transistor selected is the MJE13005 which has the following characteristics relative to this application:

BV_{ceo}	= 400V
BV_{cer}	= 700V
I_c (cont)	= 4A
h_{fe}	= 8 - 40 @ 2A
t_s	= 1.5μs
t_r	= 0.28μs
t_f	= 0.25μs

While offering inexpensive, high-voltage switching, the MJE13005 needs some support to provide adequate base drive and minimize storage time. This is readily accomplished with the circuitry shown in Figure 2. Prior to obtaining a

Fig. 2 — The high voltage power switch, Q_3, and its driver interface circuitry



start-up signal, the Drive Bias transistor in the UC3840 is off insuring that there is no quiescent current being drawn by any of this interface circuitry. At start-up, the Drive Bias switch turns on providing a pull-up for the UC3840's PWM output. The current through R16 is multiplied by the gain of Q1 to provide a forward base drive in excess of 250mA for the power switch Q3. Diodes D5 and D6 form a Baker clamp to keep Q3 out of hard saturation and improve turn-off, especially al lower collector currents.

Transistor Q2, driven on by the turn-off of Q1, provides a low-impedance path for reverse base current of Q3, and together with the use of the Baker clamp, results in a storage time for Q3 of less than 800nsec.

Snubbing circuits

There are two snubber circuits incorporated into this supply. The network of C12, D7, and R27 is used for load line shaping of transistor Q3 by delaying the voltage rise at the collector of Q3 while the current falls at turn off.

The values for the components in this network are calculated as follows:

$$C12 = \frac{I_{sc}\, t_f}{2\, V_{in\,(max)}} = \frac{2.3 \times 0.25 \times 10^{-6}}{2 \times 370} \approx 680pF$$

The resistor R27 is selected to discharge C12 with a time constant of one-half the minimum on time, which — under short circuit conditions — is approximately 2.5μs.

$$R27 = \frac{t_{on\,(min)}}{2C12} = \frac{2.5 \times 10^{-6}}{2 \times 680 \times 10^{-12}} \approx 1.8K\Omega$$

The power dissipated in this resistor is

$$P = \tfrac{1}{2}\, C12\, (V_{in\ max})^2\, f = \tfrac{1}{2}\, (680 \times 10^{-12})\, (370)^2\, 40 \times 10^3$$

$$P \approx 2 \text{ watts}$$

The second network of R26, C11, and D2 limits the voltage spike at turn off caused by the leakage inductance of the power transformer. The energy stored in this inductance is transferred into C11 via D2 after the power switch turns off and the voltage rises above the supply plus reset voltage.

C11 is defined by:

$$C11 = \frac{L_e\, I_{sc}^2}{(V_{reset} + \Delta V_{pp})^2 - V_{reset}^2}$$

Where L_e = Leakage inductance ($\approx 50\mu H$)
V_{reset} = Reset voltage across transformer (120V)
V_{pp} = Allowable leakage inductance Voltage spike (100V)

$$\therefore C11 = \frac{50 \times 10^{-6}\, (2.3)^2}{(120 + 100)^2 - 120^2} = 0.0078 \approx 10nF$$

Resistor R26 is selected to discharge C11 during the remainder of the period leaving a residual voltage equal to the reset voltage at the time turn-off next occurs.

$$R26 = \frac{(V_{reset} + \Delta V_{pp})\, 0.63\, \tau}{\Delta V_{pp}\, C11} =$$

$$= \frac{220}{100} \quad \frac{0.63\, (25 \times 10^{-6})}{(0.01 \times 10^{-6})} = 3.5K\Omega$$

In this application, R26 was increased to 4.7k due to second order effects such as reverse recovery of D2 which aids in discharging C11.

The power loss in R26 comes from the energy stored in the leakage inductance which is

$$P = \tfrac{1}{2} L_e\, I_{sc}^2\, f = \tfrac{1}{2}\, 50 \times 10^{-6}\, (2.3)^2\, 40 \times 10^3$$

$$P \approx 5.3 \text{ watts}$$

but here again, second order effects tend to reduce this value to less than 3 watts in this power supply.

Operating frequency

The frequency is set by R14 and C4 as

$$f = \frac{1}{R_T\, C_T} = \frac{1}{R_{14}\, C_4} = \frac{10^3}{12 \times 0.0022} \approx 40kHz$$

Supply start-up

The supply must reliably start with V_{DC} minimum = 250V. The value of R3 + R4 is defined by the total current requirement of the control electronics prior to start. If a start threshold of 12 volts is assumed, total control current is:

UC3840 max	= 7.0mA
R7 + R8	= 0.70mA
R10 + R11	= 0.27mA
C4 charging current	= 0.40mA
R17 + R18	= 0.22mA
Total Turn-On Current	8.59mA

$$\text{and } R3 + R4 = \frac{250 - 12}{8.59} = 27K\Omega$$

Note that R3 and R4 also provide a bleeder path to discharge C1 and C2.

Once start-up is initiated, the control current becomes:

UC3840 max	= 15mA
R16	= 6mA
Q3 Ib (x 0.375 duty cycle)	= 94mA
Total run current	= 115mA

This current must come from C3 until power is available from control winding, N4. This, in conjunction with the start-up time, defines a minimum value for C3.

Although a small soft-start capacitor is incorporated in this supply, its time constant is much shorter than the time to charge the output capacitors with the duty cycle defined by the ramp waveform and the pulse-by-pulse current limit. With the supply fully loaded, start up takes approximately 5msec. During this time, the voltage on C3 cannot fall below the under-voltage threshold.

In defining the start and UV thresholds, one other consideration is the state of the error amplifier. As defined further below, the error amplifier is going to force V_C to 12 volts. If the start threshold is set above this value, the start signal will release the soft-start clamp and arm the driver bias but no PWM output will appear until V_C droops below 12 volts and the output of the error amplifier goes high To insure soft-start action, the start threshold has been set at 11 volts and the under-voltage level is 8 volts.

Now the value for C3 can be determined from:

$$C3_{(min)} = \frac{I_{(start)}\ t_{on}}{\Delta V_C} =$$

$$= \frac{(115 \times 10^{-3})\ (5 \times 10^{-3})}{(11 - 8)} = 192\mu F$$

The start and under-voltage thresholds are defined by R7 and R8 conjunction with the 3 volt threshold and the hysteresis current of the comparator on pin 2 of the UC3840. As the voltage rises on pin2, that pin is sinking 200μA of current causing an added voltage drop across R7. When pin 2 reaches 3 volts, turn-on is initiated and — at the same time the hysteresis current is removed causing the voltage at pin 2 to jump above 3 volts.

Now, as the power supply attempts to start, the voltage on pin 2 falls and, if it reaches 3 volts from this direction, an under-voltage fault is sensed.

The start voltage at V_C is defined by:

$$V_C(start) = \frac{3V\ (R7 + R8)}{R8} + 0.2mA\ (R7) = 11V$$

while the under-voltage threshold is:

$$V_C\ (UV\ fault) = \frac{3V\ (R7 + R8)}{R8} = 8V$$

This second equation may be subtracted from the first to yeald R7 = 15KΩ, which then defines R8 -9.1KΩ.

An over-voltage fault in terms of V_{DC} can be calculated by equation:

$$V_{DC}\ (OV\ fault) = 3V\ \frac{(R5 + R6)}{R6} = 400V, \text{ or}$$

R5 = 132 R6

Small capacitors (10nF) have been added to both comparator inputs to minimize noise sensitivity.

Feed-forward

This function provides a variable-slope ramp waveform on pin 10 which is one of the inputs to the PWM comparator. This signal is compared with the output from the error amplifier on pin 1, and the pulse width is defined by the time it takes the ramp to rise to the level of the error amplifier's output. If the ramp slope is made proportional to the DC input voltage, a rising input voltage will immediately increase the ramp slope, and correspondingly reduce the pulse width with no change required from the error amplifier's output. The result will be a constant volt-second product delivered to the transformer primary resulting in good open-loop line regulation.

The design procedure used to define the ramp characteristics is to set the ramp slope such that it reaches its peak value at a time equal to the maximum pulse width allowed by the transformer design. This was set at 43% with minimum input voltage and a potential shorted output. The time for the ramp to go from its minimum to maximum value is then:

$$t_{on\ (max)} = \frac{0.43}{f} = \frac{0.43}{40 \times 10^3} = 10.75\mu sec$$

and the slope is:

$$\frac{dv}{dt}\ (min) = \frac{V_{pk} - V_{valley}}{t_{on\ (max)}} =$$

$$= \frac{4.2 - 0.5}{10.75} = 0.344V/\mu sec$$

and since the slope is determined by:

$$\frac{dv}{dt} = \frac{V_{DC}}{R15\ C8}$$

$$R15\ C8 = \frac{200V}{0\ 34V/\mu s} = 581\mu sec$$

With the knowledge that the ramp generator has greatest linearity with currents in the 100μA to 300μA range, we can pick

R15 = 1 5MΩ and C8 ≅ 390pF

Duty cycle clamp

The above analysis has provided a maximum duty cycle of 43% at minimum operating voltage When the AC line voltage is removed, however, the input voltage will fall below 200 volts with the supply still running As this voltage falls, the ramp slope will reduce and at the same time the error amplifier output will increase in an attempt to maintain regulation This could extend the pulse width beyond 43% except for the action of the duty cycle clamp divider of R19 and R20 which is set to provide 3 9V at pin 8 with V_{DC} = 200V Therefore, as V_{DC} falls, the voltage on pin 8 will also fall, taking command away from the error amplifier and maintaining a constant pulse width until the Under-Voltage sensing circuit gives a shutdown command

Voltage control

In this power supply, output voltage regulation is controlled from the primary side by sensing V_C with R10 and R11 and closing a control loop with the error amplifier and 5V reference in the UC3840 The output voltage is then

$$V_o\ (5V) = \left(\frac{N2}{N4}\right) V_{ref} \left(\frac{R10 + R11}{R11}\right)$$

Although the UC3840 optimizes this approach by the use of feed-forward which provides first-order automatic line regulation, there will still be inaccuracies caused by inadequate coupling between the windings, IR drops within the windings, and unequal losses in the rectifiers If greater voltage accuracy is required, the feedback loop must be connected directly to one of the outputs with either on optical coupler or the UC1901 Isolated Feedback Generator used to maintain isolation

The gain and phase plots for this supply are shown in Figure 3 Overall loop stability is aided by the fact that a discontinous-mode flyback topology is inherently a single pole system defined by the output load Its transfer function, excluding the error amplifier, is shown by the dashed curve of Figure 3 The DC gain from the modulator input v_C, to the output, v_O, is

$$\frac{v_O}{v_C} = K \sqrt{\frac{T R_{L\ min}}{2L_P}}$$

where K is defined by the feed-forward slope as

$$K = \frac{(\text{Max duty cycle})\ (V_{in\ min})}{\text{Ramp peak - Ramp valley}} = \frac{0\ 43 \times 200}{4\ 2 - 0\ 5}$$

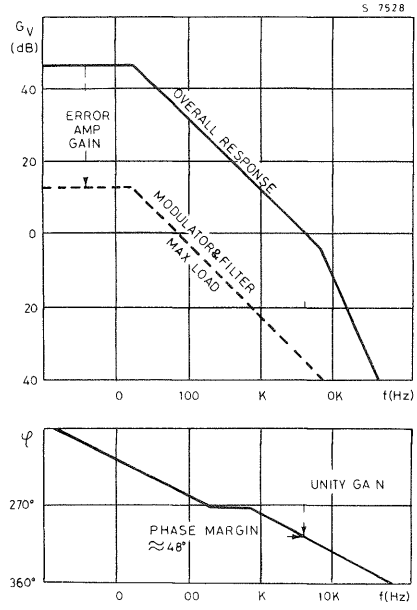
and the minimum load resistance reflected to the primary control supply is

$$R_{L\ min} = \frac{V^2}{PO\ max} = \frac{12^2}{50} = 2\ 88\Omega$$

$$\frac{v_O}{v_C} = \frac{0\ 43 \times 200}{4\ 2\ \ 0\ 5} \sqrt{\frac{25 \times 10^{6} \times 2\ 88}{2 \times 1 \times 10^{-3}}} =$$

= 4 41 = 13db

Fig 3 — Power supply loop gain and phase



The effective output capacitance, also reflected to the control supply, is

$$C_E = C14 \left(\frac{N2}{N4}\right)^2 + C13 \left(\frac{N3}{N4}\right)^2 + C3$$

,

$$= 4700 \left(\frac{4}{9}\right)^2 + 2200 \left(\frac{9}{9}\right)^2 + 200$$

= 3328μF

The yields an output pole at

$$f_1 = \frac{1}{2\pi R_L C_E} = \frac{10^6}{6.28\ (2.88)\ 3328} = 16.6\text{Hz}$$

The error amplifier is set up for an added DC gain of approximately 35db and a second pole at 8kHz - a frequency well above the overall unity gain point and yet below the roll-off frequency of the error amplifier.

Current limiting

The UC3840 limits current through the power switch, Q3, by sensing the voltage across R25. Pulse-by-pulse current limiting is defined by the divider R17, R18, and the value of R25 as:

$$I_{sc} = \frac{V_{REF}\ R18}{R25\ (R17 + R18)} =$$

$$= \frac{5.0\ (10k)}{1\Omega\ (12k + 10k)} = 2.2\ \text{amps.}$$

If the required pulse width becomes too narrow for the pulse-by-pulse circuitry to respond, the UC3840 contains a second level of protection by initiating a fault shut-down if the voltage across R25 rises to 400mV above the voltage established by R17 and R18 on pin 6. Care must be taken that this threshold is not exceeded by a leading edge spike which might be present on the current waveform.

Fault protection

The UC3840 defines four functions as faults.

1. An under-voltage signal on pin 2 (after a start command)
2. An over-voltage signal on pin 3
3. An external stop command on pin 4
4. An over current shut-down from pin 7

Any of these functions will initiate a complete shutdown of the controller with restart defined by the voltage on the reset terminal, pin 5.

If pin 5 is high or open, any fault will latch the supply off and it can only be restarted by reducing the input voltage to zero or by momentarily pulling pin 5 low. Alternatively, grounding pin 5 will cause an automatic restart after any fault shut-down.

CONSTRUCTING THE KIT

It is assumed that the user possesses reasonable electronic assembly skills and therefore detailed step-by-step instructions have not been considered necessary. Rather, a general assembly procedure is outlined below which, if followed carefully, should offer no problems. Assembly starts by properly orienting the PC board with the assembly drawing shown in Figure 5. This drawing is of the component side of the board - etch side down - with the "Warning - HighVoltage" label at the lower left hand edge.

Test and tie points

Pads have been provided on the PC board for input and output connections and for many internal test points so that complete operation of all portions of the control circuitry can be evaluated. These points are noted in Figure 5 and are listed below:

AC input	(2 pads)
DC input + 12V output	(2 pads each - note that the commons may be separated for alternate polarities)
+ 5V output	
H.V. Switching Transistor	(3 pads)

Note: 600V pulses will appear at the collector.

BE CAREFUL OF THIS TEST POINT.

Control Voltage V_C	IC pin 15
Primary Common	IC pin 13 (2 pads)
E/A Compensation	IC pin 1
5.0V Reference	IC pin 16
E/A input	IC pin 17
Drive Bias	IC pin 14
PWM Control	IC pin 12
Ramp Waveform	IC pin 10
S/S Duty Cycle Limit	IC pin 8
Oscillator Frequency	IC pin 9
C/L Limit Sense	IC pin 7
C/L Threshold	IC pin 6
Reset input	IC pin 5
Ext. Stop Input	IC pin 4
OVP Sense Input	IC pin 3
UV/Start Input	IC pin 2

No connections to these points have been included in this kit. It is suggested that the user either supply terminals or solder in small stubs or loops of bus wire so that connections to these test points can easily be made on the component side of the PC board with scope probes or other test instrumentation leads.

Jumpers

There are four jumpers required which are also not included in this kit. Use solid bus wire or a section clipped from the ends of the small resistors. These jumpers are:

AC input jumper for 110V operation
(leave out if 220 VAC is to be used)
PWM jumper to pin 12
UV/start jumper to pin 2

Reset jumper on pin 5
(leave out if it is desired to latch the supply off after any fault)

Note that there is nothing connected to pin 4. A low signal here will shut down the supply.

Small signal diodes

The seven small axial lead diodes, D2 through D8 should next be installed insuring correct polarity as shown in Figure 5.

Passive devices

Install the low-power resistors and small capacitors first. Follow with the four high-power resistors, R3, R4, R26 and R27. When inserting R26, keep the body of the resistor ≈ ¾ inch above the PC board. This resistor will get hot and it is best to have it above, rather than next to C11. At this time, the input diode bridge, D1, and the IC socket can be inserted. Note that pin 1 of the UC3840 is to the front of the PC board.

Large components

Assembly can be completed by installing the remaining components as follows:

a. Two small signal transistors, Q1 and Q2
b. Transformer
c. Electrolytic capacitors: C1, C2, C3, C13 and C14. Check polarity against signs of foil side of PC board.
d. Power transistor Q3 inserts with its front to the left, or input, inside of the PC board. Insertion is easier if the heat sink is clipped on first.

NOTE: THIS HEAT SINK IS AT THE SAME POTENTIAL AS THE COLLECTOR AND WILL HAVE UP TO 600 VOLTS PRESENT: KEEP IT CLEAR OF OTHER COMPONENTS, TEST LEADS, AND YOUR FINGERS.

e. Install the 5 volt output rectifier, D9 with its front facing the right, or output side of the board. It also gets a clip-on heat sink.

Check to see that all components are installed and match the drawing of Fig. 5 . Insert the UC3840 into the socket.

CHECKOUT PROCEDURES

With the power supply fully assembled, the following checkout procedure is recommended before any input voltage is applied. This procedure is also useful for trouble-shooting a unit which is not operating properly. Checkout will be aided if the user has installed test points at all indicated positions in the PC board. Reference should be made to Figure 5 for test point locations.

1. Insure that there is no AC input voltage applied
2. Double check all connections including diode and capacitor polarities. Insure that the UC3840 is correctly inserted into the socket.
3. Connect a minimum load on one or both outputs equivalent to 25 watts total. i.e., 2Ω on the 5V output and 12Ω on the 12V output. Be careful of the heat from these loads.
4. Install a temporary jumper shorting the base and emitter of Q3 together. Use test points provided on PC board.
5. Connect a 0 to 30 volt, 500mA lab supply to simulate the control voltage, V_C. Connect the positive lead to IC-15 and ground to IC-13. Note that IC-13 will be the ground reference point for all primary side measurements. Set V_C = Zero volts and add a 1kΩ, ½ W resistor in shunt across the power supply terminals.
6. Increase V_C to 10 volts and check the following:
   a. IC-16: should have 5V if the reference is working.
   b. IC-2: Should be 2.3V if hysteresis current is on.
   c. IC-14: Should be < 0.1V as Driver Bias is off.
7. Increase V_C to 14 volts and ckeck the following:
   a. IC-2: Should be 4.7 volts if hysteresis current is off.
   b. IC-14: Should be 12 volts with Driver Bias on.
   c. IC-9: Oscillator should show 40kHz exponential waveform.
   d. Return V_C to Zero volts but leave connected.
8. Apply the high voltage, V_{DC}. This can be done either with a DC lab supply with 300V capability or the input AC line voltage.

   A fuse rated at no more than two amps should be in series with the input line to prevent excessive damage in the event of a failure.

   NOTE: BE SURE TO USE AN ISOLATION TRANSFORMER WHEN LINE POWER IS USED AS PRIMARY GROUND IS ONE SIDE OF THE LINE.

   An AC variac will also be helpful in varying the input voltage.

   If a DC power supply is used, connect the positive line to the V_{DC} test point at the top of the board. The negative line will connect to ground on IC-13. Insure that the base-emitter short is still connected to Q3.
9. With V_{DC} = 200 volts, set V_C = 10 volts and check the following:
   a. IC-14: Should be < 0.1V if Driver Bias is off
   b. IC-8: Should be < 0.1V of Slow Start clamp is on.
   c. IC-6: Should be 2.3V to establish current limit threshold.

10. With V_{DC} = 200 volts, increase V_C to 14 volts and check the following:
    a. IC-14: Should be 12V with Driver Bias on.
    b. IC-8: Should be > 3.9V with Soft-Start clamp off.
    c. IC-10: Ramp waveform with linear rising slope extending for approximately ½ the total duty cycle. Note: scope probe input capacitance can affect this measurement.
    d. IC-1: Should be < 0.5V at output of error amplifier.
    e. IC-12: Should be still clamped to < 1.0V with no output pulses.
11. Reduce V_C to 10 volts and check the following:
    a. IC-1: Error amp output should now measure ≈ 4.1V
    b. IC-12: PWM output should have pulses of approximately 2V amplitude with a duty cycle of ≈ 40%
12. Reduce V_C to 7 volts and check the following:
    a. IC-14: Driver Bias should be off.
    b. IC-8: The soft-start clamp should be on.
13. Check the fault protective measures by following the sequence below:
    a. Start the supply by raising V_C above 14 volts and then returning it to 10 volts. Set high voltage to 200 volts. Monitor IC-12.
    b. Simulate a fault by performing each of the following, in sequence:
        (1) With an additional lab supply momentarily apply 3.5V to the OVP on IC-3, or
        (2) Again using an external supply, momentarily apply 3.0V to the current sense point, IC-7, or
        (3) Momentarily short the stop terminal, IC-4, to ground.
    c. In each case, the signal on IC-12 should case and IC-8 should clamp low.
    d. To restart the supply after a fault, V_C must go below 8 volts to reset the error latch; above 11 volts to restart; and then slightly below 12 volts to obtain a PWM output.
14. Remove all external supplies and remove the base-emitter shorting jumper on Q3. Reconnect the high voltage source and raise the voltage to obtain V_{DC} = 250 volts. The supply should be running. Q3 collector voltage can be monitored with the use of a high-voltage scope probe.

WARNING: PULSES UP TO 600V ARE ON Q3'S COLLECTOR

Normal power supply evaluation tests of line and load regulation, etc., may now be conduced.

NOTE: In experimenting with this supply, the most probable mode of failure is the shorting of the high-voltage transistor, Q3. Should this occur, transistor Q2 will also go. A two amp input fuse will normally protect the input diodes, R1, R2 and the current sense resistor, R25, although these should be checked before reapplying power. Diodes D5 and D6 are normally adequate to protect Q1 and the IC.

PARTS LIST

ICs		**Resistors**		**Miscellaneous**	
U1	UC3840N	R1, R2	1Ω, ½W	HS1, HS2	Heat Sink Thermalloy 6043
		R3	15k, 2W	T1	Transformer
Transistors		R4	12k, 2W		Coilcraft, E - 4140 - B
Q1, Q2	2N2222	R5	750k		
Q3	MJE 13005	R6	5 6k		
		R7	15k		
Diodes		R8	9 1k		
D1	VM68 Bridge	R9	unused		
D2, D6, D7	1N3614	R10	26.7k, 1%		
D3, D4	1N3612	R11	17 8k, 1%		
D5	1N4946	R12	1 5M		
D8	UES1103	R13, R14	12k		
D9	USD735	R15	1 5M		
		R16	1 5k		
Capacitors		R17	12k		
C1, C2	470μF, 250V	R18	10k		
C3	200μF, 25V	R19	750k		
C4	2200pF, 10%	R20	15k		
C5, C6	10nF, 50V	R21	33Ω, ½W		
C7	22pF	R22	15k		
C8	390pF, 10%	R23	4 7k		
C9, C10	10nF, 50V	R24	2 0k		
C11	10nF, 400V	R25	1 0Ω, 1W		
C12	680pF, 800V	R26	4 7k, 4W		
C13	2200μF, 16V	R27	1 8k, 2W		
C14	4700μF, 10V				

Fig. 4 – UC3840 PWM control circuit

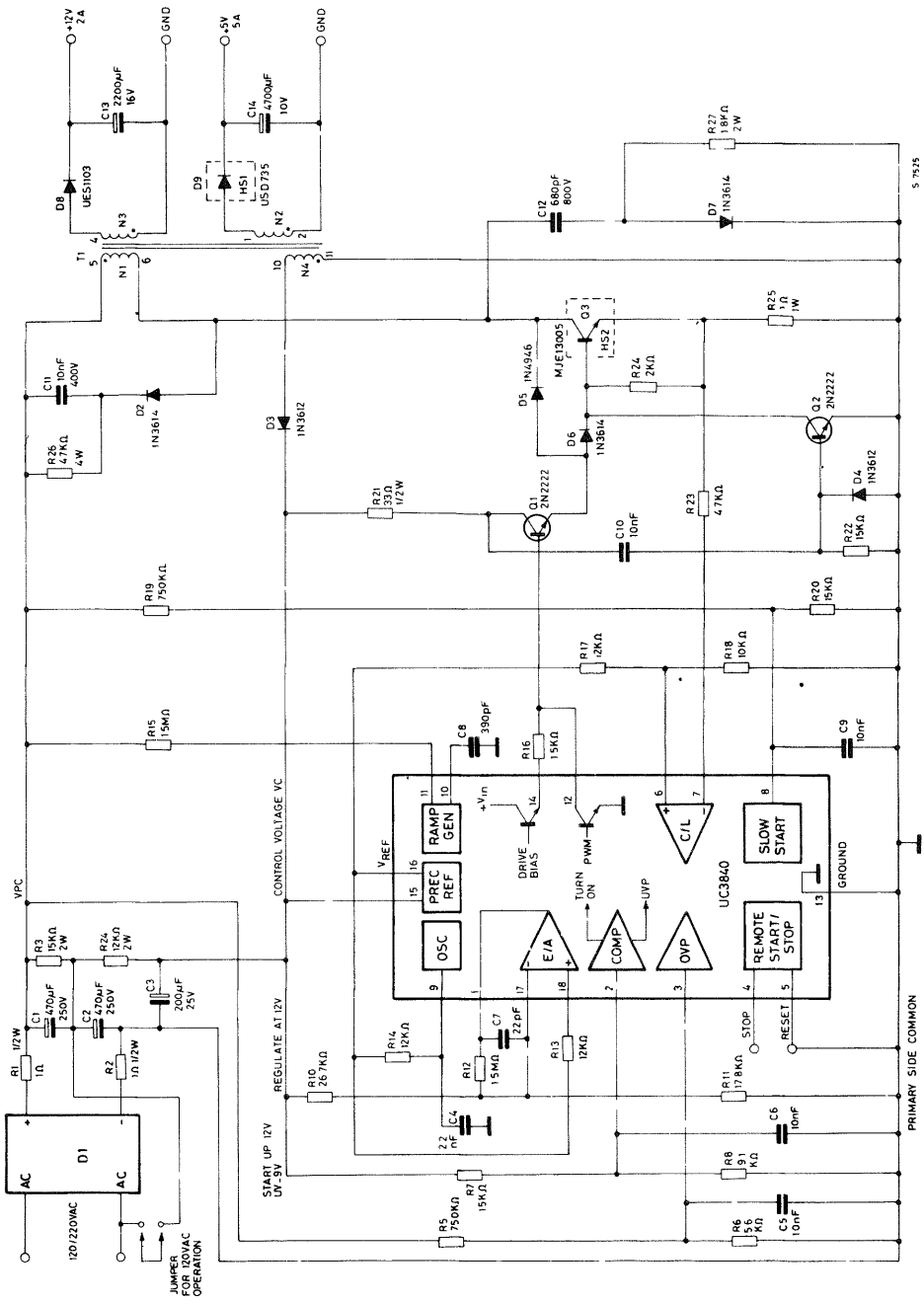
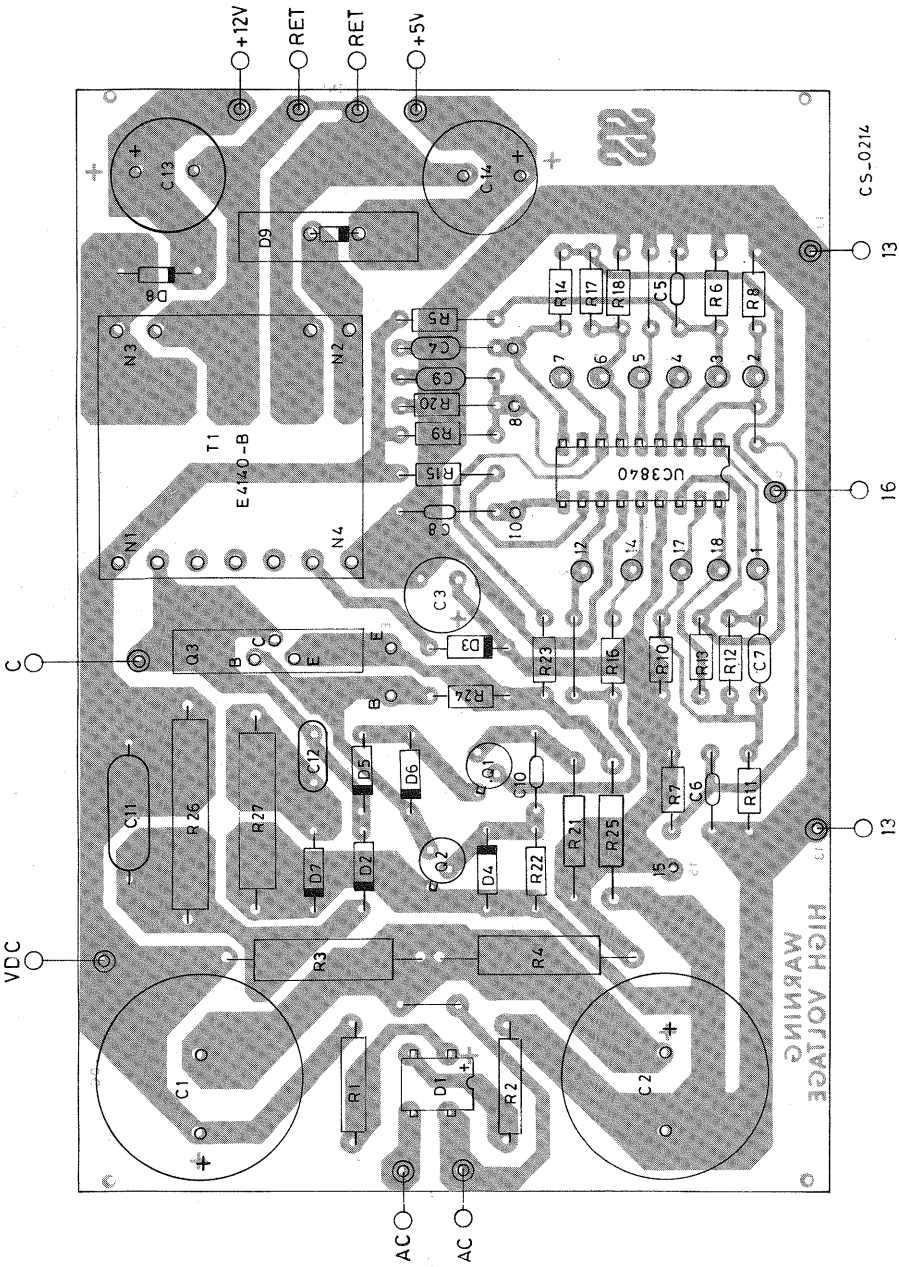


Fig. 5 — P.C. board components layout of the Fig. 4 (1 : 1 scale)



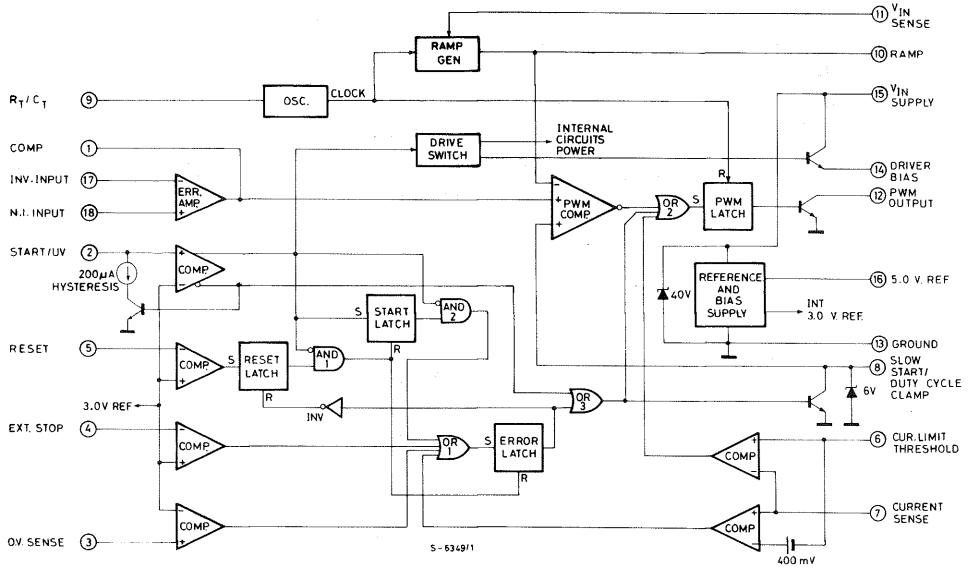
APPLYING THE UC1840 TO PROVIDE TOTAL CONTROL FOR LOW-COST, PRIMARY-REFERENCED SWITCHING POWER SYSTEMS

INTRODUCTION

There are many potential approaches to be considered in switch mode power supply design; however, the contradictory requirements of minimum cost and compatibility with ever more demanding line isolation specifications make primary control very attractive. Application of the UC1840 as a primary-side, off-line controller presents an extremely cost-effective approach to supplying isolated power from a widely varying input line while maintaining a high degree of efficiency.

Primary control means referencing all of the control electronics along with the power switching device on the input line side of an isolation transformer. An obvious advantage to this approach is the simplified interface between the control and

Fig. 1 - The overall block diagram of the UC1840, an integrated circuit optimized for primary-side control of off-line switching power supplies.



power switch. This eliminates many of the transitions across the isolation boundary which significantly increase the cost of the magnetics portion of the power supply's budget.

There are two disadvantages to primary control: (1) operating or at least starting, the control electronics from the line voltage (typically 300 VDC), and (2) providing adequate regulation (which requires feedback from the secondary across the isolation boundary). The capability of the UC1840 Control IC to solve these problems while providing all of the regulating, sequencing, monitoring, and protection functions referenced to the primary side, makes this device very attractive.

THE UC1840 CONTROLLER

The overall block diagram of the UC1840, shown in Figure 1, includes the following features:

(1) Fixed-frequency operation set by user-selected components.

(2) A variable-slope ramp generator for constant volt-second operation providing open-loop line regulation and minimizing, or in some cases even eliminating, the need for feedback control.

(3) A drive switch for low current start-up off the high-voltage line.

(4) A precision reference generator with internal over-voltage protection.

(5) Complete under-voltage, over-voltage, and over-current protection including programmable shutdown and restart.

(6) A high-current, single-ended PWM output optimized for fast turn-off of an external power switch.

(7) Logic control for pulse-commandable or DC power sequencing.

For an understanding of how these individual blocks work together in a typical, medium-power flyback power supply, reference should be made to Figure 2 and the functional description which follows.

UC1840 FUNCTIONAL DESCRIPTION

Power sequencing

A simplified schematic of the UC1840's internal power turn-on circuitry is shown in Figure 3. The key elements of this function are: (1) the Driver Bias Switch, Q3, which keeps the loading on the control voltage line, V_C, to a minimum during start up; (2) the Under-voltage Comparator which also functions as a Start Threshold Detector with programmable hysteresis; and (3) an auxiliary, primary-referenced, low-voltage winding on the main power transformer which provides normal control power after turn-on. The sequence of events is as follows:

Fig. 2 - A fully protected, isolated flyback power supply can be implemented with the UC1840, a high-voltage power switch, the transformer, and a small handful of passive components.

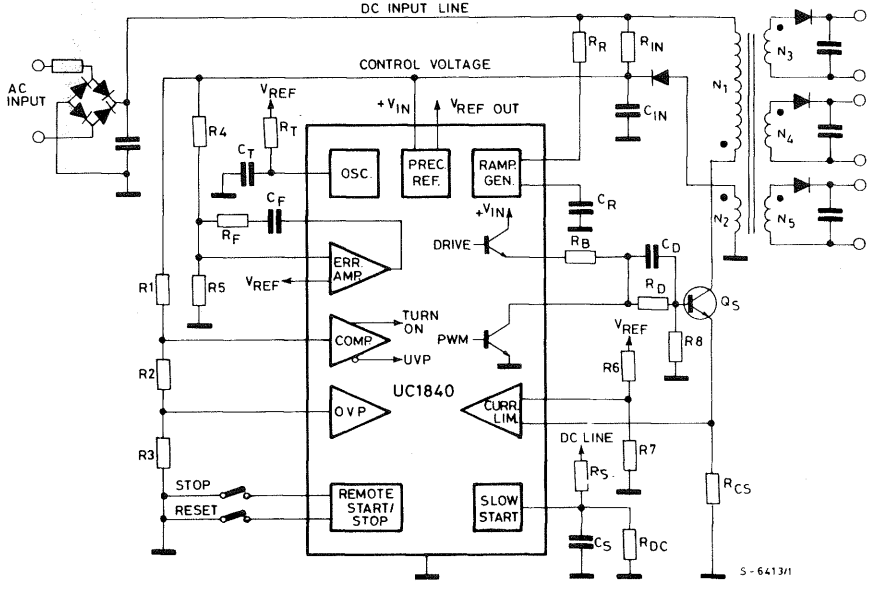
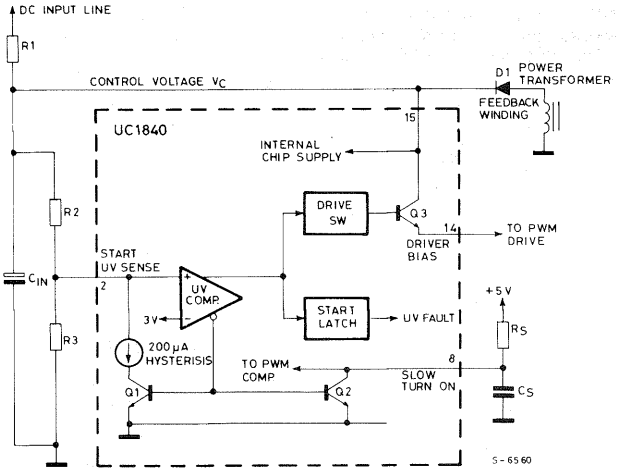


Fig. 3 - The UC1840's start circuitry requires low starting current from the DC input line with normal operating current supplied from a low-voltage feedback winding on the power transformer.



(1) While the control voltage, V_C, is low enough so that the voltage on pin 2 is less than 3V, the Start/UV Comparator does the following:

(a) A 200μA hysteresis current is flowing into pin 2 through Q1 causing an added drop across R2.

(b) The drive switch is holding the Driver Bias transistor, Q3, OFF. This insures that the only current required through R1 is the start-up current of the UC1840, plus external dividers (R2, R3, R_S, etc.).

(c) The Slow Turn-on transistor, Q2, is ON, holding pin 8 and C_S low.

(d) The Start Latch keeps the under-voltage signal from being defined as a fault.

(2) The start level is defined by:

$$V_C \text{ (start)} = 3 \left(\frac{R2 + R3}{R3}\right) + 0.2\ R2.$$

When V_C rises to this level, the Start/UV. Comparator then does the following:

(a) Turns off Q1, eliminating the 200μA hysteresis current. This allows the voltage on V_C to drop before reaching the under-voltage fault level defined by:

$$V_C \text{ (U.V. fault)} = 3 \left(\frac{R2 + R3}{R3}\right)$$

(b) Sets the Start Latch to monitor for an under-voltage fault.

(c) Activates Q3 providing Driver Bias to the power switch, pulling the added current out of C_{IN}.

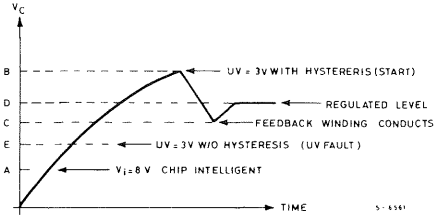
(d) Turns off Q2 allowing for programmed slow turn-on defined by R_S and C_S.

(3) A normal start-up occurs with the control voltage, V_C, following the path shown in Figure 4. If the power supply does not start, V_C will fall to an under-voltage fault which will then either initiate a restart attempt or hold the power switch off, depending upon the status of the Reset terminal as defined under Fault Sequencing. If start-up does not occur because of some fault in the Driver Bias line, V_C will continue to rise until the 40V zener across the reference circuit conducts. This will then clamp V_C to that level, protecting the control chip.

After start-up occurs, current will continue to flow in R1 providing a power loss of:

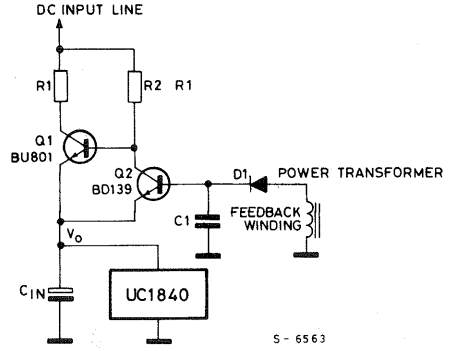
$$Pd = \frac{(V_{line} - V_C)^2}{R1}$$

Fig. 4 - Under a normal turn-on, the supply voltage to the UC1840, V_C, would rise lightly loaded to the start level, fall under the turn-on load, and then regulate at some intermediate level.



If this loss is objectionable, it can be reduced more than an order of magnitude by the addition of a two-transistor switch shown in Figure 5. In this circuit, Q1 is initially driven on by current through R2. When the feedback winding starts to conduct through D1, however, Q2 turns on leaving only R2 conducting from the input line.

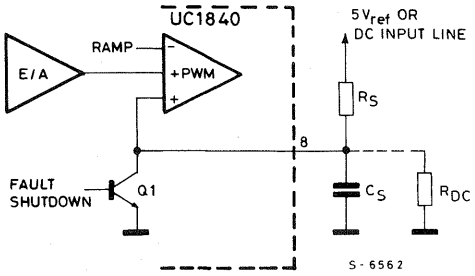
Fig. 5 - The addition of Q1 and Q2 can eliminate the steady-state current through R1 after turn-on. Q2 is selected to pass all control current through its base-emitter junction.



Slow turn-on circuit

The PWM comparator input connected to pin 8 accommodates several programming functions, shown in Figure 6. Since this comparator will only follow the lowest positive input, holding pin 8 low will effectively eliminate a PWM signal, regardless of the status of the Error Amplifier output. Prior to turn-on, and at all times when a fault has been sensed, Q1 is ON, holding pin 8 low.

Fig. 6 - Pin 8 on the UC1840 can be used for both slow turn-on and duty-cycle limiting as well as a PWM shutdown port.

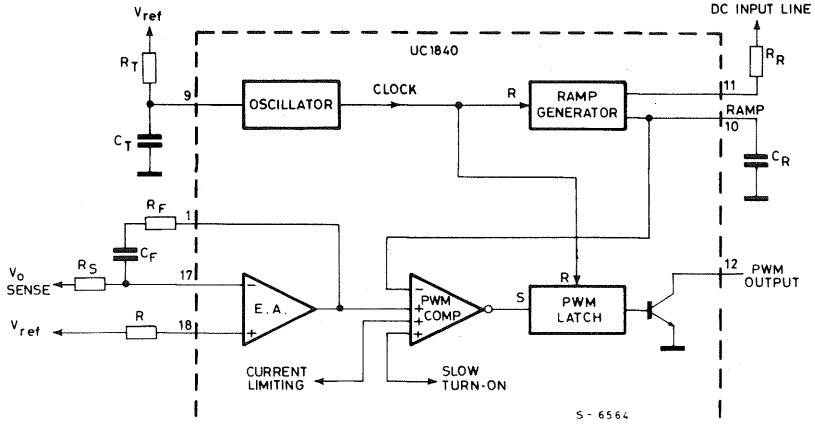


When Q1 turns off, allowing pin 8 to rise with a controlled rate will cause the output pulses to increase from zero to nominal widths at the same rate. This is accomplished by the addition of C_S and a charging source, such as R_S, to the 5V reference.

Note that where starting energy is stored in an input capacitor, the time for PWM turn-on must be less than the time required for the added Driver Bias load current to discharge the input capacitor to the under-voltage fault level. In other words, referring back to Figure 4, the slow turn-on must be faster than the time required for V_C to fall from level B to level E.

Another function of pin 8 is to establish a maximum duty cycle limit. This is achieved by clamping the voltage on pin 8 with a divider formed by adding R_{DC} to ground. If R_S is taken to the 5V reference, the clamp voltage will be fixed, which is desirable if the ramp slope is also fixed. If the ramp slope is varied with the input line – for constant volt-second operation – then the clamp voltage on pin 8 must also vary. This is readily accomplished

Fig. 7 - The pulse-width modulator within the UC1840 separates the ramp function from the fixed-frequency oscillator.



by connecting R_S to the DC input line. The divider voltage:

$$V_{Pin\ 8} = \left(\frac{R_{DC}}{R_S + R_{DC}}\right) V\ DC\ input$$

should be equal to the ramp voltage level that yields the desired maximum duty cycle, at the same DC input level.

PWM control

Pulse-Width Modulation within the UC1840 consists of the blocks shown in Figure 7. This architecture, with the possible exception of the separation between the time-base and ramp functions, is fairly conventional. It is described in greater detail in the paragraphs which follow.

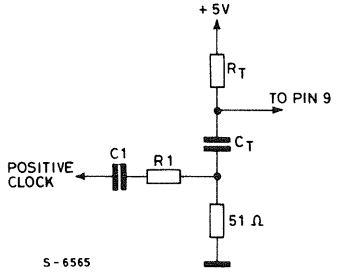
Oscillator

A constant clock frequency is established by connecting R_T from pin 9 to the 5V reference and C_T from pin 9 to ground. The frequency is approximated by:

$$f \approx \frac{1}{R_T\ C_T}$$

where the value of R_T can range from 1 kΩ to 100KΩ and C_T from 300pF to 0.1μF. The best temperature coefficients occur with C_T in the range of 1000 to 3000 pF. Although the clock output pulse is not available external to the UC1840, synchronization to an external clock can still be accomplished with the circuit of Figure 8, where R1 and C1 are selected to provide a 0.5V, 200 ns pulse across the 51Ω resistor, and R_T and C_T define a frequency slightly lower than the synchronizing source.

Fig. 8 - Synchronization to an external time base can be accomplished by adding a 51Ω resistor in series with C_T.

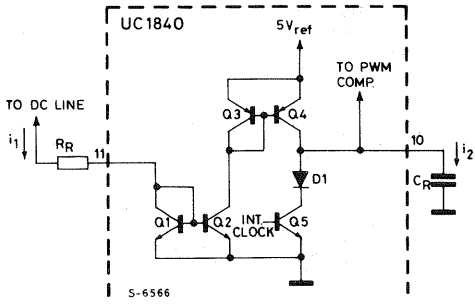


To achieve minimum start-up current, the oscillator is not activated until the input voltage is high enough to give a start command to the drive switch.

Ramp generator

The ramp generator function of the UC1840 is shown in simplified form in Figure 9.

Fig. 9 - Current mirrors Q1-Q4 are used to make the ramp charging current i_2, linearly proportional to the DC input line.



The NPN and PNP current mirrors provide a charging current to C_R of:

$$i_2 = i_1 = \frac{V_{line} - 0.7V}{R_R} \cong \frac{V_{line}}{R_R}$$

The current mirrors are useful over a current range of 1μA to 1mA, but optimum tracking occurs between 30μA and 300μA. Since the voltage across Q1 is very small, i_2 accurately represents the input line voltage. The ramp slope, therefore, is:

$$\frac{dv}{dt} = \frac{V_{line}}{R_R\ C_R}$$

The peak voltage across C_R is clamped to approximately 4.2V while the valley, or low voltage, is determined by the on-voltage of the discharge network, D1 and Q5. This is typically 0.7V.

If line sensing is not required, R_R should be connected to the 5V reference for constant ramp slope.

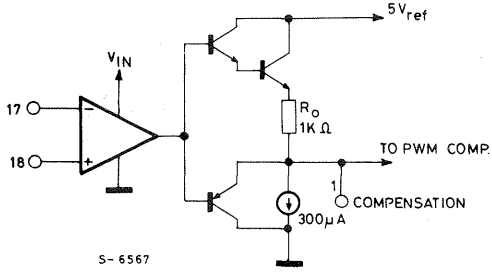
Error amplifier

This is a voltage-mode operational amplifier with an uncommitted NPN differential input stage and an output configuration as shown in Figure 10.

The 1KΩ output resistor, R_O, is used both for short circuit protection and to limit the peak output voltage to less than 4.0V so it cannot rise above the clamped ramp waveform. At sink currents less than 300 μA, the low output level will be within 200mV of ground but it rises to 1V at higher current levels.

The input common mode range is from 1V to within 2V of the input supply voltage. V_{in}, and thus either input can be connected directly to the 5V reference.

Fig. 10 - The output of the error amplifier operates class A to 300μA, but can source and sink more than 1 mA for fast response.

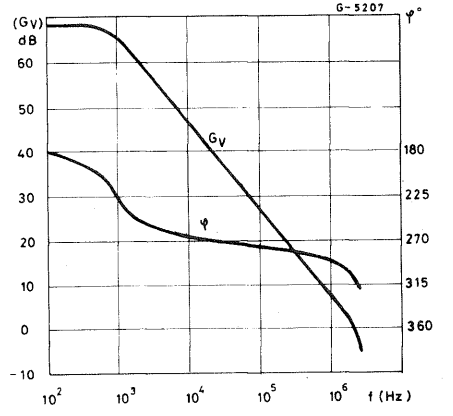


The small signal, open-loop gain characteristics are shown in Figure 11. The amplifier is unity-gain stable and has a maximum slew rate of just under 1V/μs.

PWM comparator and latch

This comparator (see Figure 7) generates the output pulse which starts at the termination of the clock pulse and ends when the ramp waveform crosses the lowest of the three positive inputs. The clock forms a blanking pulse which keeps, the maximum duty cycle less than 100%. The PWM latch insures there will be only one pulse per period and eliminates oscillation at comparator cross-over.

Fig. 11 - The UC1840 error amplifier has a DC gain of 67 dB, a 2 MHz bandwidth, and phase margin of approximately 45°.



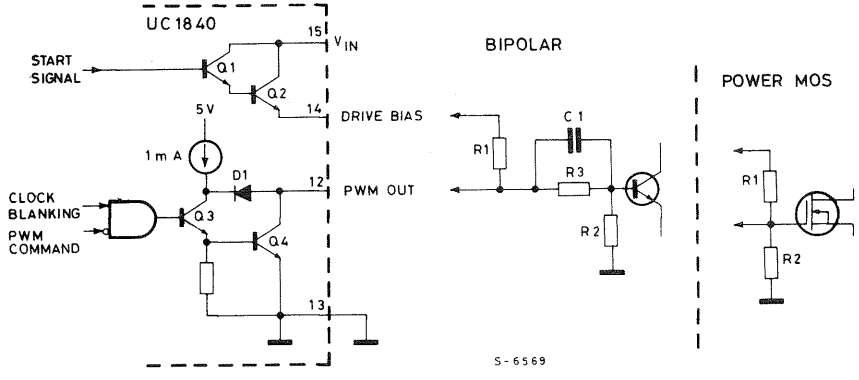
PWM output stage

In addition to the PWM output signal on pin 12, the UC1840 also includes an output gating, or arming function as Driver Bias on pin 14. Both functions should be considered together in interfacing to the external high-voltage power switch. These are illustrated in simplified form in Figure 12.

At very low input voltages (V_{IN} < 3V), both Q2 and Q4 are OFF. This may necessitate the use of R2, but its value can be high since it does not have to turn the output switch off. It merely holds it in the off state during the early portion of start-up.

Between V_{IN} = 3V and the start threshold (pin 2 = 3V with hysteresis on), Q2 is OFF and Q4 is ON, clamping the power switch off with a low impedance. A start command (UV high) turns on Q2, applying (V_{IN} - 2V) to R1. This provides a source for power switch activation; however, since Q4 is still conducting, the current through R1 is shunted to ground and the power switch remains held off.

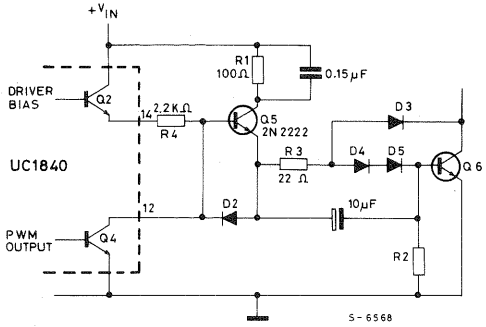
Fig. 12 - Interfacing the UC1840 PWM output stage to either Bipolar or Power MOS switches.



At the same time Q2 turns on, the clamping transistor at the slow-start terminal, pin 8, turns off allowing the voltage on pin 8 to rise according to the external slow-start time constant described earlier. This allows PWM pulses to begin to activate Q4 – narrow at first and widening to the point where the error amplifier takes command.

The interface between the UC1840 and the primary power switch may be implemented in several different ways to meet varying system requirements. One obvious application is when the use of a bipolar transistor switch requires more drive current than the Driver Bias output can provide. Figure 13 shows a more typical bipolar drive scheme where Q5 has been added to boost the turn-on current with the UC1840 still providing the high speed turn-off. The circuit now serves as a more efficient "totem-pole" driver since Q5 turns off when Q4 conducts. It also illustrates the use of a Baker Clamp to minimize storage time in Q6 and the capacitors for rapid turn-on and high-current pulse turn-off.

Fig. 13 - Adding Q5 as a switched, drive-boost transistor provides added base drive for Q6 while reducing the steady-state current through both Q2 and Q4.

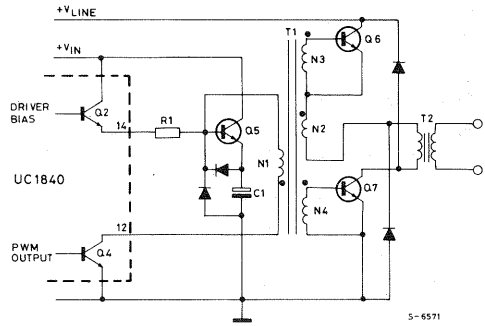


Another application is the two-transistor, off-line, forward converter topology shown in Figure 14. This circuit uses proportional base drive where the UC1840 need only supply a short, turn-off current pulse with transformer regeneration through T1 providing the steady-state drive. The magnetizing current is controlled by R1, with Q5 added to rapidly recharge C1 from which the turn-off current is supplied.

Fault protection

A significant benefit in using the UC1840 is the multi-faceted fault-sensing and programming capability built into the device. With the intent to provide complete control to the power system under all types of potential malfunctions, fault-sensing circuitry has been included to sense over-voltage, under-voltage, or over-current conditions. Additionally, high-speed, pulse-by-pulse digital current limiting is included as a separate function. The operation of these circuits is described below.

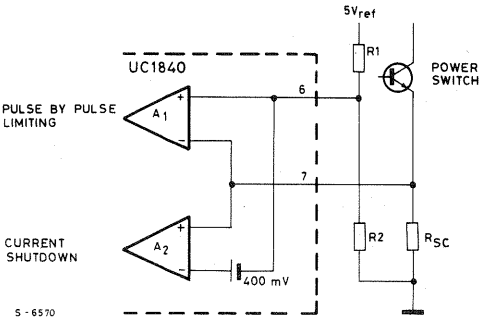
Fig. 14 - Interfacing the UC1840 single PWM output to a two-transistor off-line forward converter which uses proportional base drive.



Current limiting

The current limit comparators have differential inputs for noise rejection but are intended to be used with ground-referenced current sensing as in Figure 15. Comparator A1 is delegated to pulse-by-pulse current limiting. The output of this comparator drives the PWM comparator, where it activates the PWM latch, terminating each pulse when the current sensed by R_{SC} reaches a threshold defined by divider R1, R2, and the 5V reference.

Fig. 15 - Current limiting and overcurrent shutdown are implemented with comparators of different thresholds and a single current sense resistor.



Since V_C is intended to track the supply's output voltage, the addition of a resistor from pin 6 to V_C will provide some foldback to the current limit characteristic. Since comparator A1 has zero offset voltage, it is activated when the voltage across R_{SC} equals that across R2. Comparator A2, with an offset voltage of 400 mV, will activate for over-current shutdown when the voltage across R_{SC} rises to 400 mV higher than the voltage across R2. Since the input bias to both comparators is less than 5 μA, a low-pass filter for noise rejection may be inserted between R_{SC} and the sense inputs. Activation of comparator A2 is defined as an over-current fault and it triggers the Error Latch. Its operation follows.

Fault sequencing

The fault sequencing logic of the UC1840 is shown in Figure 16. Since a fault is defined by this device as an activation of the Error Latch, it makes sense to start here in an attempt to understand this portion of the circuitry. Setting the Error Latch immediately turns on Q1 and Q2, discharging the slow-start capacitor and terminating the PWM output. Note that there is an additional path from the inverted output of the Start/UV comparator through OR2 which keeps pin 8 low. This is to keep the slow-start low during initial turn-on which is not intended to be classified as a fault.

The input to the Error Latch is from OR1 which triggers on signals resulting from four possible events:

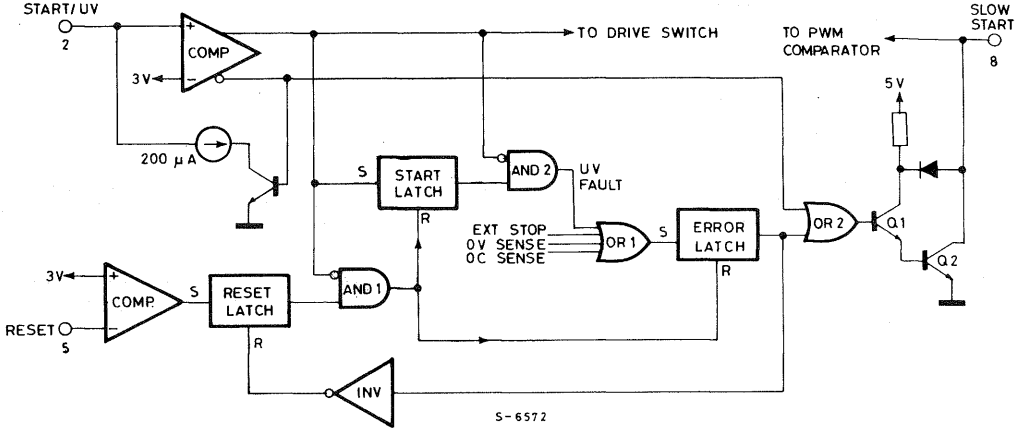
(1) A voltage less than 3V (after prior turn-on) at the Start/UV sense terminal, pin 2.

(2) A voltage greater than 3V at the Over-Voltage Sense terminal, pin 3.

(3) A voltage of less than 3V on the Ext. Stop terminal, pin 4.

(4) An over-current signal resulting in a differential voltage between pins 7 and 6 of greater than 400 mV.

Fig. 16 - Fault sequence logic is designed to insure a complete shutdown and fully controlled restart upon any of four possible fault conditions.



Any of these inputs need only be momentary to set the Error Latch. Transient protection may be necessary to eliminate false triggering, but it can be readily accomplished as all the comparator inputs are high impedances requiring less than 2 μA of input current, and the 3.0V reference yields a high noise immunity.

The Start Latch can be understood by recognizing that at initial turn-on it is reset with a low output. This prevents AND2 from transmitting a UV fault signal from the Start/UV non-inverting output to the Error Latch. At the start voltage level, defined by a high level on the Start/UV non-inverting output, the Start Latch sets but AND2 still provides no output. Only when the Start/UV input goes low again, with the Start Latch output held high, will AND2 yield an output into the Error Latch.

The status of the Reset terminal, pin 5, determines what happens after the Error Latch is set. The choices are:

(1) Latch off and require a recycle of input voltage to restart.

(2) Continuously attempt to restart.

(3) Attempt some number of restarts and then latch off.

(4) Latch off and await a momentary reset pulse to restart.

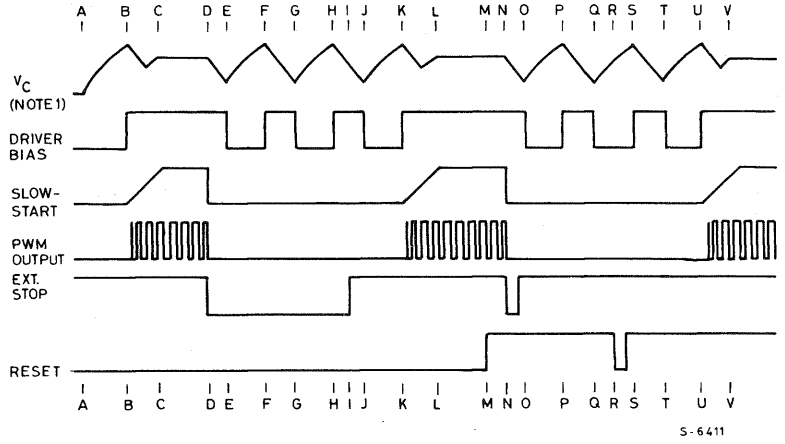
To examine the operation of the Reset Latch, note that prior to setting the Error Latch, its low output is inverted to hold the reset input to the Reset Latch high. This forces the Reset Latch's output low, regardless of the voltage on pin 5, and, thus, insures no signal out of AND1. With the setting of the Error Latch, the Reset Latch is free to take the

state commanded by pin 5: high if pin 5 is low and vice-versa. The latch allows merely a pulse to set the Reset Latch; the voltage on pin 5 need not be steady state.

With a high Reset Latch output, the Error Latch still does not reset until a low signal is sensed on the Start/UV sense terminal. At that point, AND1 then resets both the Error Latch and the Start Latch re-establishing the initial conditions for a normal start after fully charging the input capacitor. Of course, if the fault is still present, when the Start/UV input reaches the start level terminating the Error Latch reset signal, this latch will immediately set again.

To aid in the understanding of this logic, Figure 17 gives a pictorial representation of its operation with both steady-state and momentary signals on both the Ext. Stop and Reset terminals.

Fig. 17 - The interrelationship between the functions controlled by the fault sequence logic is illustrated with both static and pulse commands on the ext. stop and reset terminals.



Note 1: V_C represents an analog of the supply output voltage generated by a primary - referenced secondary winding on the power trasformer. It is the voltage monitored by the start/UV comparator and in most cases is the supply voltage V_{IN} for the UC1840.

TIME	EVENT
A	INITIAL TURN-ON V_C RISES WITH LIGHT LOAD.
B	START THRESHOLD DRIVER BIAS LOADS V_C.
C	OPERATING PWM REGULATES V_C.
D	STOP INPUT SETS. ERROR LATCH TURNING OFF PWM.
E	UV LOW THRESHOLD. ERROR LATCH REMAINS SET.
F	START TURNS ON DRIVER BIAS BUT ERROR LATCH STILL SET.
G	V_C AND DRIVER BIAS CONTINUE TO CYCLE.
H	
I	STOP COMMAND REMOVED.
J	ERROR LATCH RESET AT UV LOW THRESHOLD.
K	START THRESHOLD NOW REMOVES SLOW-START CLAMP.
L	RETURN TO NORMAL RUN STATE.
M	RESET LATCH SET SIGNAL REMOVED.
N	ERROR LATCH SET WITH MOMENTARY FAULT.
O	ERROR LATCH DOES NOT RESET AS RESET LATCH IS RESET.
P	V_C AND DRIVER BIAS RECYCLE WITH NO TURN-ON.
Q	
R	RESET LATCH IS SET WITH MOMENTARY RESET SIGNAL.
S	V_C MUST COMPLETE CYCLE TO TURN ON.
T	START AND ERROR LATCHES RESET.
U	NORMAL START INITIATED.
V	RETURN TO NORMAL RUN STATE.

If Driver Bias turn-on is used to pump an increment of charge into an integrating capacitor, and that capacitor voltage is applied to the Reset Terminal, some number of retrys could be programmed to take place before the Reset voltage rises to 3V, which would then lock the output OFF. Since Driver Bias continues to cycle in the latched-off state, the Reset terminal will remain high until it is either remotely pulled low or the input voltage to the controller is interrupted.

Note that an important element in any restart after a shutdown is the lowering of the voltage at the Start/UV terminal below its UV threshold. While this will occur normally in bootstrap-driven applications, this device can also be used with a constant driving voltage by externally applying a momentary pull-down signal to the Start/UV input after a fault shutdown.

CONCLUSION

With the UC1840, power supply designers now have a device specifically developed for off-line, primary control and one which has addressed the problems of operation under less than "ideal" or normal conditions. Not only does this device make it easier to comply with stringent isolation requirements by requiring a minimum of communication between primary and secondary, but it is also ideally suited for powering systems in remote locations where only a simple transmitted pulse is available for power sequencing.

250W OFF-LINE FORWARD CONVERTER DESIGN REVIEW

This paper gives a practical example of the design of an off-line switching power supply with forward converter topology. Topics include transformer and filter inductor design, proportional base drive, component selection, output filter design and closing the control loop using the new UC1524A control circuit.

POWER SUPPLY SPECIFICATIONS:

Topology:	Forward Converter with Proportional Base drive	
Line input:	117V ± 15%	(99-135V), 60Hz
	230V ± 15%	(195-265V), 50Hz
Output:	Voltage:	5V
	Current:	5 to 50A
	Current Limit:	60A Short Circuit
	Ripple Voltage:	100mV P-P Max.
	Line Regulation:	± 1%
	Load Regulation:	± 1%
Other Features:	Efficiency:	75%
	Line Isolation:	3750V
	Switching Frequency:	40kHz

THE COMPLETE POWER SUPPLY CIRCUIT

The complete 250W switching power supply schematic is given in Figure 2. This supply meets all of the specification requirements defined on this page.

Fig. 1 – Block diagram of the switching power supply

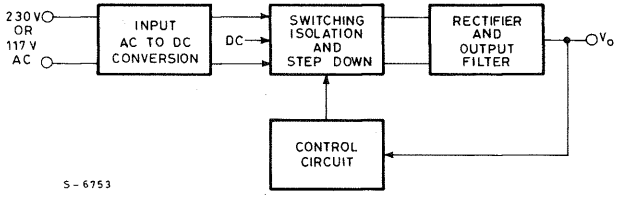
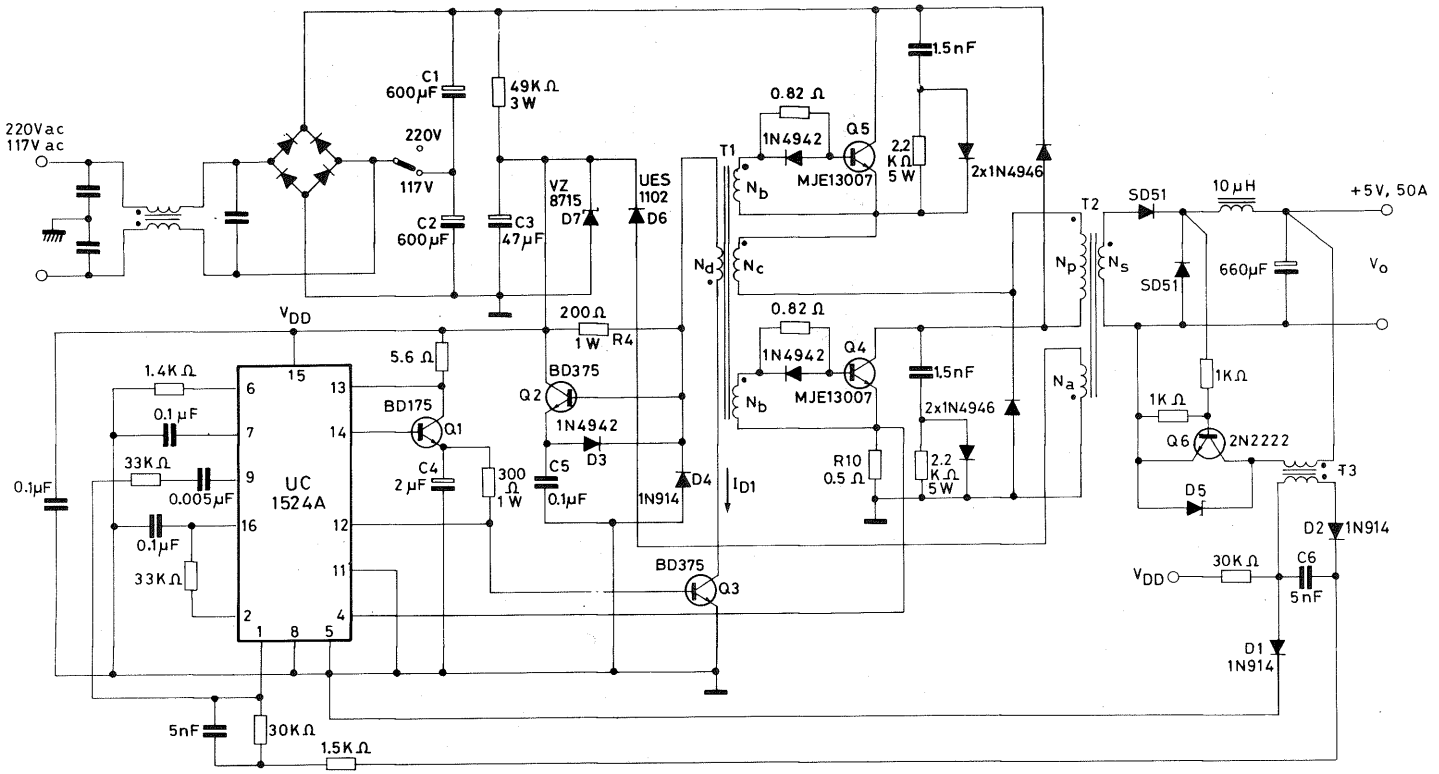


Fig. 2 - Complete 250W switching power supply



LINE INPUT AC TO DC CONVERSION

The input rectifier/filter section converts the AC line voltage into a crudely filtered and unregulated DC voltage, V_{in}, which powers the downstream switching regulator. The input section is configured as a full-wave bridge when operating from the 230V line, and as a voltage doubler when operated from 117V. This provides approximately the same V_{in} range (200-380V) for the switching regulator with either line voltage. Minimum input voltage, V_{min}, is 200V at low line.

The design of the input section is covered extensively in Appendix B. The power input required in this application equals power output (250W) divided by efficiency (75%), or 333W. Circuit values for this application can be obtained by multiplying the 100W input values given in Table 1 of Appendix B by $P_{in}/100 = 3.33$, using the worst case voltage double configuration:

$$C_1 = C_2 = 3.33(160) = 533\mu F \text{ (use } 600\mu F) \quad (1)$$

$$I_{chg} = 3.33(1.126) = 3.75A \text{ RMS AC} \quad (2)$$

The switching regulator draws 40kHz rectangular current pulses which discharge the input capacitors. Peak discharge current, i_{dis}, occurs at V_{min} when the duty cycle, D, is maximum (50%):

$$i_{dis} = P_{in}/(V_{min}D) = 333/(200 \cdot 0.5) = 3.33A \text{ peak} \quad (3)$$

The RMS AC component of the discharge current, I_{dis}, which flows through the input capacitors at worst case 50% duty cycle is:

$$I_{dis} = (i_{dis})/2 = 3.33/2 = 1.67A \text{ RMS AC} \quad (4)$$

The total RMS AC current rating required for the input capacitors is calculated from Equation 6 of Appendix B.

$$I_{CAP} = \sqrt{I_{chg}^2 + I_{dis}^2} = \sqrt{3.75^2 + 1.67^2} \quad (5)$$

SWITCHING CIRCUIT TOPOLOGY

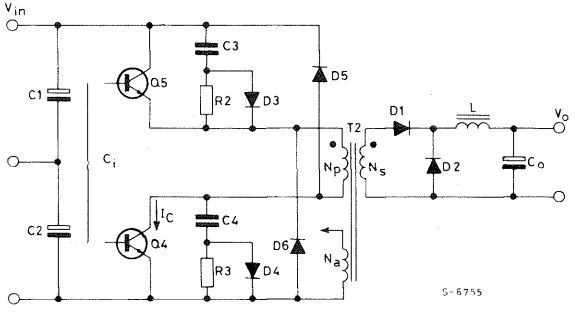
The two transistor forward converter configuration shown in Figure 3 was used in this 250W switching power supply for the following reasons:

1. Transistor voltage ratings are half the voltage required in a comparable single transistor circuit (400V vs. 800V). Only 1/4 the silicon chip area is required for the same current rating, and the switching speeds will be twice as fast.
2. The snubber networks are for load line shaping only and are not required to absorb all the energy stored in the transformer leakage reactance. Instead, clamp diodes D_5 and D_6 conserve most of this energy by returning it to the input, improving the efficiency.
3. Closed-loop stability is easier to achieve than with a flyback converter because there is no right half plane zero.
4. Filter capacitor requirements are much less severe than in boost or flyback converters because of the output filter inductor.
5. Transformer construction is simplified because there is no need for a clamp winding (N_a is used for the auxiliary supply).
6. Reliability is improved because faster transistors dissipates only one half of these reduced losses.

Disadvantages of this topology are:

1. Two transistors are required instead of one (but cost may be less).
2. Restricted to less than 50% duty cycle to permit core reset. This results in poorer transformer utilization.
3. Added cost of filter inductor, which is not required for the flyback converter.

Fig. 3 - Two transistor forward converter



SPECIFYING THE SWITCHING TRANSISTORS

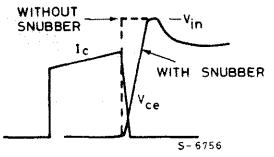
Maximum peak primary current flowing through the transistors, I_{CM}, is the same as i_{dis} from Equation 3 or 3.33A.

The transistors should have good $V_{CE(sat)}$ and switching speeds at a collector current of at least 4.0A, which includes an allowance for unusual conditions such as short circuit current. (Disregard spec sheet "maximum current ratings" which are inflated for competitive marketing reasons, and focus on the specified test conditions).

The collector voltage rating must be greater than maximum V_{in}, or 380V in this application. Conservatively, this should be the BV_{CEO} rating, but with careful load line shaping to make certain the transistor is completely off before voltage is applied, a less conservative designer might specify BV_{CEX} greater than $V_{in(max)}$.

The MJE13007 satisfies the above requirements, with BV_{CEO} of 400V, $V_{CE(sat)}$ less than 2.0V at 5A, and worst case fall time of 400ns under the proportional base drive conditions provided.

Fig. 4 - Effected of snubber network on turn-off characteristics



POWER TRANSFORMER DESIGN

The design of the 40kHz inverter transformer is detailed in Appendix A. A primary to secondary turns ratio of 148/9, or 15.33, ensures that 5V output is provided with minimum V_{in} of 200V at 50% duty cycle, including voltage drops in rectifiers, transistors and windings.

Transformer winding N_a is used to provide an auxiliary supply to power the control and base drive circuits. This makes good use of the energy stored in the transformer primary inductance.

SNUBBER NETWORK DESIGN

The turn-off snubber networks shown across each transistor in Figure 3 provide shaping of the load line to ensure that it remains below the reverse bias safe operating area (RBSOA) of the transistors. Capacitors C_3 and C_4 accomplish this by holding the voltage across each transistor low during current turn-off. The snubber capacitors thus absorb the turn-off transistion energy that otherwise would have been dissipated in the transistors (see Figure 4).

(6)

$$C_3 = C_4 = \frac{I_{CM}\, t_f}{2\, V_{in\,(max)}} = \frac{3.33 \times .4 \times 10^{-6}}{2 \times 380} = .00175\mu F \text{ (use } .0015\mu F)$$

Resistors R_2 and R_3 are designed to discharge the snubber capacitors with a discharge time constant of one-half the minimum on time, $t_{on(min)}$.

(7)

$$t_{on(min)} = \frac{D_{(max)}}{f}\,\frac{V_{in\,(min)}}{V_{in\,(max)}} = \frac{0.5}{40.000}\,\frac{200}{380} = 6.58\mu s$$

$$R_2 = R_3 = \frac{t_{on\,(min)}}{2C_3} = \frac{6.58 \times 10^{-6}}{2 \times 1.5 \times 10^{-9}} = 2.2K\Omega$$

Maximum power dissipation in each resistor:

$$P_{R2} = P_{R3} = \frac{1}{2} C_2\, V_{in(max)}^2\, f \qquad (8)$$

$$= \frac{1.5 \times 10^{-9}}{2} \times 380^2 \times 40.000 = 4.3W$$

OUTPUT FILTER DESIGN

The output filter and its associated waveforms are shown in Figure 5. The filter inductor calculation is based on the maximum "off" time:

$$D_{(min)} = D_{(max)}\,\frac{V_{in\,(min)}}{V_{in\,(max)}} = 0.5\,\frac{200}{380} = .263 \qquad (9)$$

$$t_{off(max)} = \frac{1 - D_{(min)}}{f} = \frac{1 - .263}{40.000} = 18.4\mu s \qquad (10)$$

The inductance required to prevent discontinuous mode operation depends upon the minimum load current:

$$\Delta I_{L(max)} = 2I_{o(min)} = 2 \times 5 = 10A \qquad (11)$$

(12)

$$L = \frac{(V_o + V_F)\, t_{off(max)}}{\Delta I_{L(max)}} = \frac{(5 + 0.6)\, 18.35}{10} = 10\mu H$$

The capacitance required to achieve the output ripple specification of 0.1V is:

(13)

$$C_o = \frac{1}{2}\,\frac{\Delta I_{L(max)}}{2}\,\frac{1}{2f}\,\frac{1}{v_o} = \frac{10}{8 \times 40.000 \times 0.1} = 312\mu F$$

The maximum ESR of the capacitor is:

$$ESR = v_o/\Delta I_{L(max)} = 0.1/10 = .01\Omega \qquad (14)$$

Fig. 5 – Output power filter design

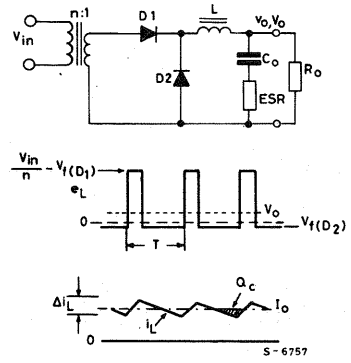
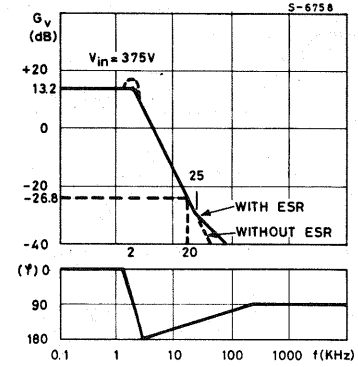


Fig. 6 – Control to output transfer function LC filter and modulator



To obtain the necessary ESR requires a capacitor much larger than the 312μF calculated. This design will use three 220μF solid tantalum capacitors, Mallory THF227MO10P1G, in parallel. A single 14.000μF aluminium electrolytic capacitor, Mallory CG0143M10R2C3PL could also be used.

With the tantalum capacitor, the resonant frequency of the filter is 2kHz. With the aluminum electrolytic, the resonant frequency is reduced to 425Hz, changing the closed-loop design.

CLOSING THE CONTROL LOOP

The UC1524A is used for the control circuit. It has additional features such as pulse by pulse current limiting and high current and voltage output capability (200mA, 60V) compared with the SG1524. The UC1524A reference is trimmed to ± 1% which makes it possible to avoid using a voltage-setting potentiometer in many instances.

The control to input transfer function, dV_o/dV_c, shown in Figure 6, incudes the cascaded gain of the sawtooth modulator within the UC1524A control IC, the power switching circuit, and the output filter characteristics, $H_e(s)$.

In the control IC, a control voltage V_C is compared with sawtooth ramp voltage V_S (2.5V) to establish the drive pulse width to the power switches. For the forward converter, only one of the two alternating outputs of the UC1524A is used so as to limit the duty cycle to 50% maximum and allow for transformer core reset:

$$D = 0.5V_c/V_s = 0.5V_c/2.5 = V_c/5 \qquad (15)$$

The forward converter is a member of the buck regulator family. Transformer turns ratio n = 16.44:

$$V_o = \frac{V_{in}}{n} D = \frac{V_{in}\ V_c}{n\ 2V_s} \qquad (16)$$

The low frequency control to output transfer characteristic is obtained by differentiating with respect to V_C:

$$\frac{d\ V_o}{d\ V_c} = \frac{V_{in}}{n\ 2V_s} = \frac{380}{15.33 \times 5} = 4.95 = 13.2db \qquad (17)$$

Note that gain is greatest at maximum V_{in}. The overall control to output transfer characteristics including the filter is:

$$\frac{d\ V_o}{d\ V_c} = \frac{V_{in}}{n\ 2V_s} = H_e(s) \qquad (18)$$

The filter introduces a two-pole characteristic at its resonant frequency (2kHz). Above resonance, the gain drops 40db per decade, and the phase shift becomes -180 degrees. Combined with the -180 degees phase shift of the feedback network, this will cause instability and oscillations unless compensated.

Closing the loop involves feeding back the error voltage from the output terminal of the supply ($\hat{v}_o$) to the IC control voltage port ($\hat{v}_c$) through the UC1524A error amplifier. The approach taken is to make the gain of the feedback network such that the overall loop gain crosses zero db (with adequate phase margin) at one half the switching frequency.

As shown in Figure 6, control to output gain is 13.2db at low frequencies, rolling off above 2kHz at -40db per decade, so that at 20kHz the control to output gain is 13.2 -40, or 26.8db. For overall loop gain of zero, the feedback network gain must be made +26.8db at 20kHz.

From 20kHz down to 2kHz, there is a net single zero in the feedback network which cancels one of the two filter poles and reduces the phase shift in this region to -270 degrees.

Below the filter resonant frequency the two filter poles are gone. However, the resonant frequency may be less than 2kHz because of plus tolerances on the filter capacitor. The feedback network is therefore designed to transition from a net single zero to a single pole at 1kHz, half the resonant frequency.

Fig. 7 - Open loop gain and phase plot

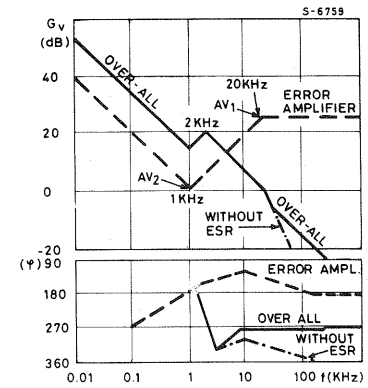
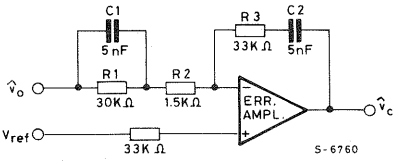


Fig. 8 - Error amplifier with compensation



ZEROS: $R_1 C_1$ – 1kHz
$R_3 C_2$ – 1kHz
POLES: $R_2 C_1$ – 20kHz
ERROR: AMPL. – 10Hz

Figure 7 shows the gain and phase plot of the error amplifier and the overall feedback loop. Figure 8 shows the specific feedback network used to achieve this result.

The high frequency error amplifier gain is set by R_2 and R_3. An R_3 value of 33k is chosen to minimize amplifier loading:

$$Av_1 = R_3/R_2 = 26.8db = 21.9 \quad (19)$$

$$R_2 = R_3/Av_1 = 33000/21.9 = 1500\Omega$$

The required error amplifier gain at 1kHz is:

$$Av_2 = Av_1 \times 1kHz/20kHz = 21.9 \times 1/20 = 1.095\,(0.8dB) \quad (20)$$

The gain at 1kHz is determined by R_1, R_2 and R_3:

$$Av_2 = R_3/(R_1+R_2) = 33K/(R_1+1500) = 1.095 \quad (21)$$

$R_1 = 28.6K\Omega$ (use $30K\Omega$)

The two zeros at 1kHz which changes the feedback network from a net single zero to single pole are equal to:

$$f_1 = \frac{1}{2\pi\ R_1\ C_1} = \frac{1}{2\pi\ R_3\ C_2} = 1kHz \quad (22)$$

$C_1 = 5.3nF, \quad C_2 = 4.8nF$

C_1 and R_1 in parallel with R_2 result in an additional pole at 20kHz. This flattens the error amplifier gain above 20kHz. The overall phase shift will gradually increase toward 360 degrees, but it doesn't matter because the overall gain is less than one.

An additional pole occurs below 10Hz. This is the inherent single-pole characteristic of the error amplifier's $5M\Omega$ output impedance loaded by feedback capacitor C_2.

PROPORTIONAL BASE DRIVE

In Figure 2, transistors Q_2 and Q_3 and base drive transformer T_1 provide proportional drive to the bases of power switching transistors Q_4 and Q_5. The proportional base drive technique provides excellent performance from high voltage bipolar transistors. It provides large base current pulses for fast turn-on and turn-off, but with modest drive power requirements. Sustaining base drive is provided regeneratively from a collector current winding on the drive transformer. The transistors are never overdriven, even under light load conditions, since the sustaining base drive is proportional to the collector current. Design considerations for the proportional base drive technique are given in Appendix C.

Referring to the circuit of Figure 2, when Q_3 is on, R_4 establishes 75mA magnetizing current in drive winding N_d of T_1. When Q_3 turns off, the energy stored in T_1 drives 150mA into the base of each transistor. Collector current starting to flow in N_c provides sustaining base drive. With I_C of 3.33A under full load conditions, an additional 667mA of drive is provided to each base.

While Q_3 is off, capacitor C_5 charges through Q_2 in less than $1\mu s$. Then, when Q_3 turns back on, C_5 provides a negative base drive pulse of -1.5A to each transistor, achieving turn-off in less than $1\mu s$.

Drive transformer T_1 has a drive winding inductance of 0.7mH and is designed to saturate at 75mA. High voltage insulation is not required because all windings are on the line side of the supply.

Core: Ferroxcube 1107P-L00-3B7 Pot Core
N_d: 20 turns AWG34 (0.16mm.)
N_b: 5 turns AWG28 x 2 (2 wires, one for each base)
N_c: 2 turns 5 x AWG28 (5 wires paralleled, AWG28 = 0.32mm.)

AUXILIARY POWER SUPPLY

A 15V auxiliary supply powers the control and driver circuits, obtaining its energy from capacitor C_3. Flyback energy is normally provided by T_2 through winding N_a and D_6 to maintain the charge on C_3 every switching cycle. However, at initial power-up it is necessary to provide separate means to activate the V_{dd} supply. Otherwise, the control and driver circuits could not become functional and the supply could not start to switch.

The unique under-voltage lockout feature of the UC1524A facilitates this technique. All of its internal circuits are disabled (except the reference) until the V_{dd} voltage reaches 8V. This holds the standby current to less than 4mA until the 8V threshold is reached, and permits C_3 to be initially charged through R_1 from the unregulated input. Enough energy is stored in C_3 to operate the control/drive circuits for several switching cycles, until flyback energy from winding N_a can take over and maintain the voltage on C_3.

It is also necessary to eliminate base drive to Q_3 during initial power-up, otherwise Q_3 will draw current through R_4 which will prevent C_3 from initially charging. This is accomplished by transistor Q_1 which disconnects base drive source capacitor C_4. When the UC1524A becomes active, its second output turns Q_1 on periodically to charge C_4.

The amount of energy stored in the power transformer is twice the drive/control circuit requirements. Excess energy is dumped into 15V zener diode D_7 which establishes the V_{dd} supply voltage at that level. This also provides a constant clamp voltage across the switching transistors, regardless of line voltage. With good coupling between N_a and primary winding N_p, it may be possible to eliminate clamp diodes D_{12} and D_{13}.

OUTPUT VOLTAGE SENSE AND OVER-CURRENT SENSE

A small, inexpensive transformer, T_3, couples the output voltage to the line side control circuit with high voltage isolation. The transformer is wound on a Ferroxcube 204-T250-3E2A ferrite toroidal core. Primary and secondary windings are both 14 turns 0,2mm.

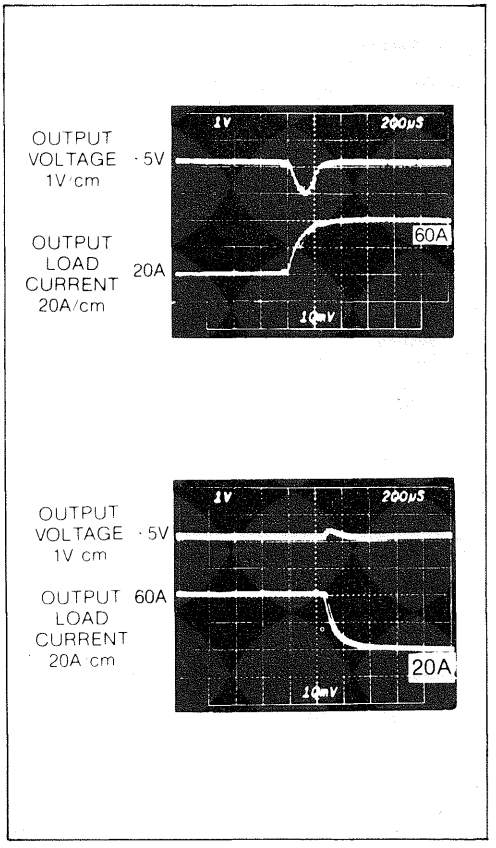
During the time the power switching transistors are on, Q_6 is on, applying V_o to the primary of T_3. Through D_2, this provides a real-time feedback voltage to the control circuit across C_6. When Q_6 is off, D_5 clamps the flyback voltage to 15V. Core reset is accomplished well before the end of the "off" time, since the "off" time of the forward converter is always more than 50%. All transformer windings then go to 0V, establishing a DC coupling level. D_1 in series with the ground return compensates for the forward voltage drop and temperature coefficient of D_2.

Pulse by pulse current limiting is set by sense resistor R_{10}. Primary current is limited to 4A, corresponding to 62A load current.

Transient response of the switching supply is shown in Figure 9 with changes in load from 20A to 60A and back to 20A. This behavior is a large signal phenomenon. It doesn't matter how fast the control loop is, it is temporarily driven into the bounds because the load change is much larger than the output filter inductor current can accomodate in one cycle. Nevertheless, recovery is smooth and there is no evidence of ringing or oscillations, demonstrating the stability of the control loop. Step changes in load current that are small enough for the control loop to remain functional are barely noticable at the output.

Transient response can be improved by reducing the filter inductor and increasing the filter capacitor size, but this will increase the minimum load current required to keep the inductor current from becoming discontinuous.

Fig. 9 - Step change in output load



APPENDIX A
DESIGN OF THE POWER TRANSFORMER AND FILTER INDUCTOR

Flux Density Excursion

In this forward converter application, the flux excursion is entirely within the first quadrant of the B-H characteristic, from zero flux density toward saturation. With simple duty cycle control, using the UC1524A control IC, it is possible to have nearly twice the normal Volt-seconds, $V_{in(max)}$ $t_{on(max)}$, during startup or after a large step increase in load current. This means that the flux density cannot be permitted to go more than half way toward saturation under normal conditions or the core will saturate under transient conditions.

Saturation flux density for 3C8 power ferrite material is greater than 0.3 Tesla (3000 Gauss), allowing a ΔB of 0.15T (0 to 0.15T) in this application. (With Volt-second control, available in the UC1840 control IC, a ΔB of 0.3T would be permissible, significantly reducing the transformer size).

Core Selection

The core area product, AP, requirements in this applications are calculated for power input of 333 watts and frequency of 40kHz.

$$AP = A_W A_e \left(\frac{11.1\ P_{in}}{K\ \Delta B\ f}\right)^{1.143} = \left(\frac{11.1\ 333}{0.141\ 0.15\ 40.000}\right)^{1.143} = 5.4\ cm^4$$

This equation is based on the assumptions that the windings occupy 40% of the window area, the primary and secondary windings are of equal area, and the windings are operated at a current density that will result in a temperature rise of 30°C with natural convection cooling.

The EC52 core with an AP of 5.71 cm^4 is the obvious choice.

Designing the windings

The minimum number of primary turns required to support the volt-seconds required for normal operation is calculated from equation:

$$N_{p(min)} > \frac{5000\ V_{in(min)}}{\Delta B\ \ Ae\ \ f} > \frac{5000\ 200}{0.15\ 1.83\ 40.000} > 91\ turns$$

The primary to secondary turns ratio is:

$$n = \frac{N_p}{N_s} = \frac{0.9D\ (V_{in(min)} - V_{CE(sat)})}{V_o + V_F} = \frac{0.45\ (200 - 2)}{5 + 0.8} = 15.36$$

Secondary turns:

N_s = Integer (Np/n) = Integer (91/15.36) = 6 turns

Recalculate the primaty turns:

$N_p = 6 \times 15.36 = 92$ turns

RMS primary current from:

$$I_p = I_{in(max)}/K_t = \frac{P_{in(max)}}{V_{in(min)}\ K_t} = \frac{333}{200\ \ 0.71} = 2.34A$$

The maximum current density for this size core is:

$$J_{max} = 450AP^{-.125} = 450(5.71)^{-.125} = 362\Omega/cm^2$$

The minimum primary wire area, Axp. is:

$A_{xp} = I_{p(max)}/J_{max} = 2.34/362 = .0065\ cm^2$

0,9mm is appropriate.

The maximum RMS secondary current, I_s, occurs at 50% duty cycle:

$I_{s(max)} = I_{o(max)}/1.414 = 50/1.414 = 35.3A$

Minimum secondary wire area, A_{xs}, is:

$A_{xs} = I_{s(max)}/J_{max} = 35.3/362 = 0.0975\ cm^2$

This calls for 3,6mm to 3,25mm. Ten 1mm wires in parallel will carry the required secondary current and provide a smooth winding with less leakage inductance and acceptable eddy current losses. Copper strip 2.5 x 0.4 cm could also be used.

The number of turns required for the auxiliary winding is:

$$N_a = \frac{V_{dd}\ N_p}{V_{in(min)}} = \frac{15\ \ 92}{200} = 7\ turns$$

This will provide enough volt-seconds during flyback to reset the core (back to zero flux density) at 50% maximum duty cycle. 0,2mm wire is adequate to carry the V_{dd} supply current. This winding should be tightly coupled to the primary.

Double-check the wire fit in the window (neglect N_a). The total copper area of all windings should be less than 40% of the total window area of the core (0.4 x 3.12 = 1.25 cm^2 max).

$A_W' > N_p A_{xp} + N_s A_{xs} = 92(.0065) + 6 \times 10(.00823) = 1.09\ cm^2$

Calculate Losses and Temperature Rise

The mean length per turn, ℓ_t, for the EC52 core is 7.3 cm, and 0.9mm wire is .000353Ω/cm at 100°C.

$P_W = 2\ell_p^2\ N_p\ \ell_t\ (\Omega/cm) = 2(2.34)^2 \times 92 \times 7.3 \times .000353 = 2.59W$

The flux density assumes the transformer is operating with a symmetrical flux swing about the origin. The forward converter operates asymmetrically with $\Delta B/2$, or .075T. The resulting 0.1W/cm^2 must be multiplied by the core volume to obtain the total core loss, P_c.

$P_c = .01 \times 18.7 = .187W$

Total transformer losses are:

$P_t = P_w + P_c = 2.59 + .187 = 2.78W$

The temperature rise of the core for natural convenction cooling is calculated from:

$$\Delta\Theta = \frac{850\ P_t}{A_s} = \frac{850\ \ (2.78)}{91} = 25.9°C$$

Summarizing the transformer design:

Core: Ferroxcube EC52, 3C8 Ferrite E-E core
N_p: 92 turns 0,9mm
N_a: 7 turns 0,2mm
N_s: 6 turns 10 x 1mm (10 wires paralleled)

The primary and auxiliary windings are tightly coupled. The secondary is insulated with 2 mil mylar tape to provide 3750V line isolation capability.

Filter Inductor Design

The inductor design is summarized as follows:

Core: Ferroxcube 4229-3C8 Ferrite Pot Core
Winding: 7 turns 10 x 1.15mm (10 wires paralleled)
Losses: 2.2W
Temp. Rise: 35°C

APPENDIX B
LINE INPUT AC TO DC CONVERSION AND INPUT FILTER CAPACITOR SELECTION

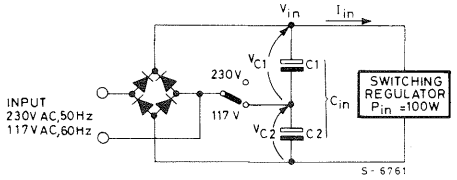
The input rectifier/filter section of an off-line power supply converts the 50-60Hz AC line voltage to a DC voltage, V_{in}, which powers the downstream high frequency switching section. A circuit diagram typical of a dual range input rectifier/filter section is shown in Figure 1B. For 230V line operation, the input rectifiers are configured as a full-wave bridge. For 117V operation, the input circuit is reconfigured as a voltage doubler, so that V_{in} will be approximately the same as under 230V operation. While it is technically possible to operate the input section as a bridge at both 230V and 117V, the switching regulator would have to be designed to operate over a much larger V_{in} range which would significantly increase its cost.

Table 1 - 100W Input Rectifier/Filter Section

Parameters		117V BRIDGE (60Hz)	117V DOUBLER (60Hz)	230V BRIDGE (50Hz)	Unit
RMS Line Voltage	V_{ac}	99-135	99-135	195-265	V
Peak Line Voltage	V_{pk}	140-191	280-382	276-375	V
Max Ripple Voltage	V_r	40	80	76	V
DC Input Voltage	V_{in}	100-191	200-382	200-375	V
Input Capacitance	* C_{in}	203	80	61	μF
Doubler Capacitance	* C_1, C_2	—	160	(122)	μF
Charging Time	t_c	1.954	2.275	2.345	ms
Peak Charge Current	* i_{chg}	3.64	3.28	1.82	A
RMS AC Charge Current	* I_{chg}	1.54	1.126	.771	A

* For power levels other than 100W, multiply capacitance and current values by $P_{in}/100$ ($P_{in} = Po/\eta$).

Fig. 1B - Circuit diagram



Input filter capacitance C_{in} determines V_r, the 100/120Hz peak to peak ripple voltage component of V_{in} (see Figure 2B). At low line voltage, V_r determines the minimum input voltage, V_{min}, which is an important consideration in the design of the switching supply. V_{min} defines the transformer turns ratio required to achieve the specified output voltage at maximum duty cycle.

If the input filter capacitance is too small, the resulting large ripple voltage will require increased duty cycle range and control loop gain to maintain the specified output voltage. V_{min} will be less, resulting in poor transformer utilization, higher peak current through the switching transistors, and higher peak inverse voltage across the output rectifiers.

Input filter capacitance larger than necessary will not only cost more, the recharging current pulses drawn from the line will be narrower and larger in amplitude (Figure 2B). This hurts the line power factor and increases EMI. The higher RMS input current causes increased losses in the line, input rectifiers and filter capacitors, and can impair reliability.

A reasonable rule of thumb is to compromise on a ripple voltage 25-30% of the minimum peak line voltage, resulting in acceptable capacitor size, weight and cost. Table 1 shows the resulting values for 117V bridge operation with V_{min} of 100V, and 117V doubler and 230V bridge operation with V_{min} of 200V, for a switching supply with 100W power input. The input filter capacitors are designed to supply the full load energy of the supply and hold V_{in} above the desired V_{min} between AC line peaks. With the switched dual range input section (117V doubler of 230V bridge) filter capacitor requirements are determined by the voltage doubler configuration.

Design Equations and Calculations:

The following examples are given for full-wave bridge operation from the 230V line (195-265V), and full-wave bridge and voltage doubler operation from the 117V line (99-135V).

Since virtually all the losses in the switching power supply are downstream of the input rectifier/filter, the input section must handle the entire power input, P_{in} (equal to full load power output divided by efficiency). Power input in these examples is assumed to be 100W at full load. The resulting capacitance and current values can be adjusted for any other power input by multiplying by the actual $P_{in}/100$.

Between line peaks, the input filter capacitor must supply the entire full load energy requirement of the supply. Ripple voltage V_r must be small enough to maintain V_{in} greater than the desired V_{min} under worst case conditions of low line frequency, low line voltage and full load. Energy required at 100W for one entire line cycle at **50Hz** (worst case used with 230V line):

$$V_{in} = \frac{P_{in}}{f} = \frac{100}{50} = 2.0 \text{ Joules (W-sec.)} \qquad (1)$$

At **60Hz**, the energy required for one line cycle at 100W is reduced to **1.667 Joules**.

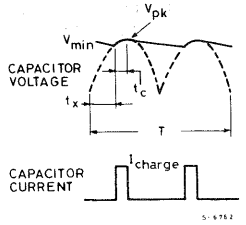
Full Wave Bridge Operation

Referring to Figures 1B and 2B, input filter capacitor C_{in} (C_1 in series with C_2) charges to peak line voltage each half cycle. C_{in} then discharges, providing all the energy required by the switching supply until it is recharged at the next half cycle. Energy from C_{in} each **half** line cycle is:

$$W_{in/2} = \frac{1}{2} C_{in} (V_{pk}^2 - V_{min}^2) \qquad (2)$$

$$C_{in} = \frac{V_{in}}{V_{pk}^2 - V_{min}^2}$$

Fig. 2B - Bridge waveforms



As show in Figure 2B, the recharging time, t_c, is established by the intercept of the capacitor voltage waveform with the rectified AC line:

$$V_{min} = V_{pk} \cos(2\pi f t_c) \qquad (3)$$

$$t_c = \frac{\cos^{-1}(V_{min}/V_{pk})}{2\pi f}$$

Assuming a rectangular charging current pulse of peak amplitude i_{chg} (constant current during the charging interval):

$$\Delta Q = i_{chg} \Delta t = C \Delta V \qquad (4)$$

$$i_{chg} = C (V_{pk} - V_{min})/t_c$$

The RMS AC component of the charging current, I_{chg}, is conducted through the filter capacitors and contributes to capacitor heating due to their equivalent series resistance (ESR). The DC component of the total RMS charging current does not pass through the capacitor and does not contribute to capacitor heating.

$$I_{chg} = \sqrt{I_{CHG}^2 - I_{DC}^2} = \sqrt{i_{chg}^2\, t_c\, 2/T - i_{chg}^2\, (t_c\, 2/T)^2} \quad (5)$$

$$I_{chg} = i_{chg} \sqrt{t_c\, 2f - (t_c\, 2f)^2}$$

The switching supply discharges the input capacitors by drawing high frequency pulses of current. The AC component of the RMS discharge current, I_{dis}, also causes filter capacitor heating. The filter capacitors must be selected to have RMS current ratings greater than the total RMS AC current components. This is an important consideration for capacitor reliability.

$$\text{Total } I_{CAP} = \sqrt{I_{chg}^2 + I_{dis}^2} \quad (6)$$

The DC component of the high frequency discharge current pulses equals the DC component of the charging current from the line. Because the form factor of the high frequency discharge current at low line is much better (closer to 1.0) than the charging current waveform, the RMS AC discharge current, I_{dis}, is much less than I_{chg}, depending somewhat on the switching circuit topology.

For 230V (50Hz) bridge operation: At 195V minimum line voltage, the minimum peak voltage, V_{pk}, is 276V. Conservatively assume 270V peak, allowing for drops in rectifiers and line. From Equation (2):

$$C_{in} = \frac{2}{270^2 - 200^2} = 61\mu F$$

Charging pulse width from Equation (3):

$$t_c = \frac{\cos^{-1}\ (200/270)}{2\pi\ 50} = 2.345\text{ms}$$

Peak charging current from Equation (4):

$$i_{chg} = 61\,(270\text{-}200)/2.345 \times 10^{-3} = 1.82\text{A}$$

RMS charging current from Equation (5):

$$t_c\, 2f = 2.345 \times 10^{-3}\ 2\ 50 = .2345$$

$$I_{chg} = 1.82 \sqrt{.2345 - .2345^2} = .771\text{A}$$

For 117V (60Hz) bridge operation (normally used only for single range 117V input): At 99V minimum V_{pk} is 140V. Conservatively assume 135V peak, allowing for drops in rectifiers and line:

$$C_{in} = \frac{1.667}{135^2 - 100^2} = 203\mu F$$

$$t_c = \frac{\cos^{-1}\ (100/135)}{2\pi\ 60} = 1.954\text{ms}$$

$$i_{chg} = 203(135\text{-}100)/1.95 \times 10^{-3} = 3.64\text{A}$$

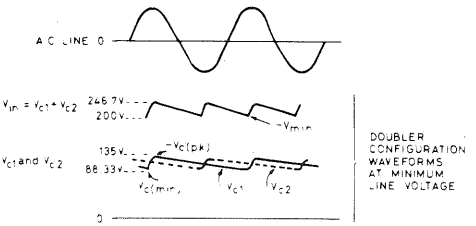
$$t_c\, 2f = 1.954 \times 10^{-3} \times 2 \times 60 = .2345$$

$$I_{chg} = 3.64 \sqrt{.2345 - .2345^2} = 1.54\text{A}$$

Voltage Doubler Operation, 117V (60Hz) Line:

Referring to Figure 1B and 3B at minimum line voltage (99V), the peak voltage is 140V. Conservatively assume 135V peak, allowing for drops in rectifiers and line.

Fig. 3B - Voltage doubler waveforms



C_1 and C_2 alternately charge to peak line voltage. Note that whenever the input voltage, V_{in}, is at instantaneous minimum, one capacitor is at its minimum, but the other capacitor is half way between peak and minimum voltage. The minimum voltage on each capacitor corresponding to an overall V_{min} of 200V can be approximated as follows:

$$V_{min} = V_{C1min} + V_{C2avg} = V_{Cmin} + \frac{V_{Cmin} + V_{Cpk}}{2}$$

$$V_{Cmin} = \frac{2V_{min} - V_{Cpk}}{3} = \frac{2(200) - 135}{3} = 88.33\text{V} \quad (7)$$

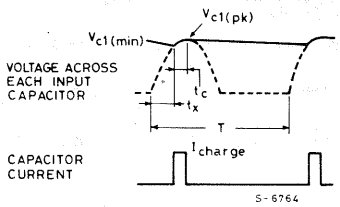
C_1 and C_2 each discharge for a complete cycle. Each capacitor must supply half the energy required by the switching regulator for an entire line cycle:

$$W/2 = \frac{1}{2}\ C_1\ (V_{Cpk}^2 - V_{Cmin}^2)$$

$$C_1 = C_2 = \frac{W}{V_{Cpk}^2 - V_{Cmin}^2} = \frac{1.667}{135^2 - 88.33^2} = 160\mu F \quad (8)$$

C_{in} the series combination of C_1 and C_2, equals $80\mu F$

Fig. 4B - Voltage doubler charging current



Note that the voltage doubler operated from the 117V line requires larger C_{in} than the 230V bridge input, so that for supplies with dual range 117/230V input, the 117V doubler operation dictates the filter capacitor requirements.

Figure 4B shows the waveforms associated with charging each of the input capacitors in the voltage doubler configuration at full load and minimum line voltage. Recharge time, t_c, is established by the intercept of the capacitor voltage waveform with the rectified AC line:

$$V_{C1min} = V_{C1pk} \cos(2\pi f t_c)$$

$$t_c = \frac{\cos^{-1}(V_{C1min}/V_{C1pk})}{2\pi f} \quad (9)$$

$$t_c = \frac{\cos^{-1}(88.3/135)}{2\pi\ 60} = 2.275 \text{ ms}$$

Assuming a rectangular charging current pulse of peak amplitude i_{chg} (constant current during the charging interval):

$$\Delta Q = i_{chg}\,\Delta t = C\,\Delta V$$

$$i_{chg} = C(V_{pk} - V_{min})/t_c \quad (10)$$

$$i_{chg} = 160(135 - 88.3)/2.275 \times 10^{-3} = 3.28A$$

The RMS current in each capacitor is:

$$I_{chg} = i_{chg}\sqrt{t_c f - t_c f^2} \quad (11)$$

$$t_c f = 2.275 \times 10^{-3} \times 60 = .1365$$

$$I_{chg} = 3.28\sqrt{.1365 - .1365^2} = 1.126A$$

APPENDIX C
PROPORTIONAL BASE DRIVE

Proportional base drive is a simple and effective method of achieving improved performance with high voltage bipolar power switching transistors in off-line applications. As shown in Figure 1C, a current transformer provides regenerative base drive current whose amplitude is proportional to the collector current being switched. The drive current ratio is established by the turns ratio of the collector and base windings.

The proportional drive method may be employed with any power switching circuit topology. Advantages over conventional fixed base current drive methods include:

1. Fixed base drive current must be large enough to handle the full load (or short-circuit load) collector current. Under lightly loaded conditions, the switching transistors are severely overdriven, resulting in long storage and fall times and more difficult turn-off. Proportional drive provides optimal performance under varying load current conditions.
2. Proportional base drive requires less drive power from the control circuit. During the "on" time of the switching transistor, base drive is provided regeneratively from the collector circuit through the current transformer. The control drive circuit is not required to provide sustaining base drive current. It must only provide short pulses of drive current to initiate turn-on and turn-off. The amplitude of these drive current pulses can easily be made large enough to obtain good switching performance from high voltage bipolar devices in off-line applications.

Referring to Figure 1C and 2C, when driver transistor Q_1 is on, power switch Q_2 is off. Magnetizing current I_{d1} in the control drive winding N_d approaches a steady-state value equal to the drive circuit supply voltage V_{dd} divided by R_1. Capacitor C_1 is discharged and there is zero voltage across all windings of T_1.

Fig. 1C - Proportional base drive circuit

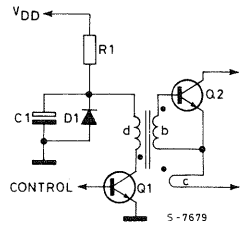
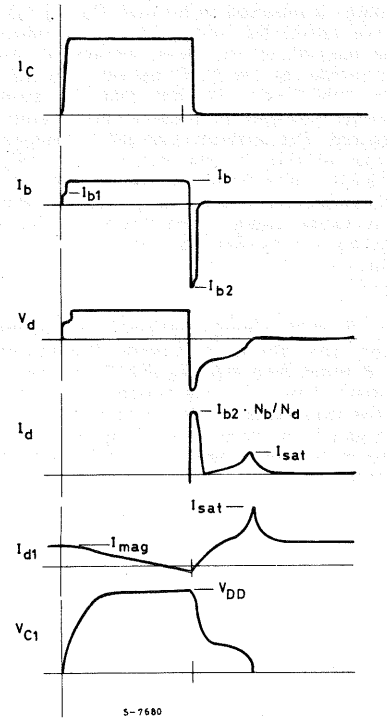


Figure 2C - Waveforms



When the output of the control circuit turns on, driver Q_1 turns off and primary current I_{d1} must cease. Energy stored in T_1 causes the voltage at the dotted ends of all windings to flyback in the positive direction. I_{d1} multiplied by turns ratio N_d/N_b becomes I_{b1}, the turn-on base drive current pulse to Q_2.

Collector current I_c starting to flow in winding N_c causes a regenerative increase in base drive to Q_2 until it is switched fully on. The final value of I_c induces a proportional base drive current, I_b, according to the turns ratio N_b/N_c.

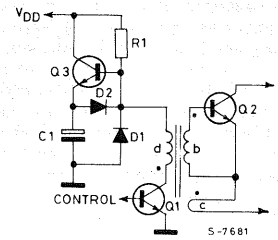
During the time that Q_2 in on and Q_1 is off, capacitor C_1 charges through R_1 to supply voltage V_{dd}. At the end of this "on" period, driver transistor Q_1 is turned on again, applying the voltage on capacitor C_1 to the drive transformer primary. This drives the voltage on the base of Q_2 sharply negative. The turn-off base current pulse, I_{b2}, can be made larger than Q_2 collector current, resulting in very rapid turn-off of Q_2.

After Q_2 is off and I_{b2} ceases, any remaining voltage on C_1 across the drive transformer primary helps to rebuild the magnetizing current. Diode D_1 prevents the possibility of any underdamped ringing from driving the upper end of N_d negative. At the end of the "off" period, magnetizing current I_{d1} has been re-established and the cycle repeats.

It is quite feasible to operate high voltage bipolar transistors at frequencies above 50kHz with reasonable efficiency because of the large amplitude base drive pulses obtainable with this method. However, the circuit of Figure 1C, as just described, is not capable of operation at frequencies above a few kHz. This is because capacitor C must charge to V_{dd} during the "on" period of Q_2, and the R_1 C_1 charging time constant is far too long for this to be accomplished at 50kHz.

This problem is solved by the addition of a rapid recharge circuit as shown in Figure 3C. During the time that Q_2 is on and Q_1 is off, current through R_1 is multiplied by the current gain of Q_3, which significantly reduces the charging time of C_1. When Q_1 turns on, C_1 discharges through D_2. The base-emitter of Q_3 is reverse biased, holding it off during the entire Q_2 "off" time.

Fig. 3C - Improved proportional base drive circuit



Design Procedure:

Application parameter values must be defined, including drive requirements for the power switching transistors.

I_c	Maximum collector current
I_{b1}	Initial turn-on base drive current
I_c/I_b	Sustaining proportional base drive ratio
I_{b2}	Turn-off base drive current at max. I_c
V_{bb2}	Turn-off base drive source voltage at max I_c
t_2	Maximum transistor turn-off time
V_{dd}	Drive circuit supply voltage
f	Operating frequency

Drive transformer base/collector turns ratio is equal to the desired proportional base drive ratio:

$$N_b/N_c = I_c/I_b \quad (1)$$

Drive transformer driver/base turns ratio is established by the desired turn-off base source voltage and drive circuit supply voltage, minus 1V diode drop:

$$N_d/N_b = (V_{dd}-1)/V_{bb2} \quad (2)$$

When Q_1 turns off, primary magnetizing current, I_{d1}, transferred to the base winding must provide the required turn-on base drive, I_{b1}.

$$I_{d1} = I_{b1}/(N_d/N_b) \quad (3)$$

The R_1 value required to obtain this magnetizing current is:

$$R_1 = V_{dd}/I_{d1} \quad (4)$$

During initial turn-off, driver primary current I_{d2} must absorb the proportional base drive current and transformer magnetizing current I_{d1} in addition to the turn-off base drive current:

$$I_{d2} = \frac{I_{b2} + I_c/(N_b/N_c)}{(N_d/N_b)} + I_{d1} \quad (5)$$

Capacitor C_1 is designed to supply the worst-case energy required to turn off Q_2:

$$W = \frac{1}{2} C_1 (V_{dd}-1)^2 = (V_{dd}-1)\, I_{d2}\, t_2$$

$$C_1 = \frac{2\, I_{d2}\, t_2}{V_{dd}-1} \quad (6)$$

When Q_2 is operated at very low duty cycle (such as immediately after a sudden decrease in load current), C_1 may not have time to fully charge to V_{dd} during the vary short "on" time, in spite of the assistance provided by Q_3. This will probably not be a problem, because Q_2 will also not have time to store much charge and will be much easier to turn-off. The time required for Q_2 to reach equilibrium charge storages is comparable to the time required to remove this charge during turn-off. The C_1 charging time constant (reduced according to the gain, H_{fe} of Q_3) will generally be adequate if it is less than 1/2 the Q_2 turn-off time, t_2.

$$T_{C1} = R_1\, C_1/H_{fe} \quad (7)$$

Drive Transformer Design:

Turns ratios for the drive transformer were established in equations (1) and (2). Only certain integral number of turns are permissible for each winding. For example, if N_d/N_c is 25, the permissible number of drive winding turns are 25, 50, 75, etc., corrensponding to 1, 2 and 3 collector turns.

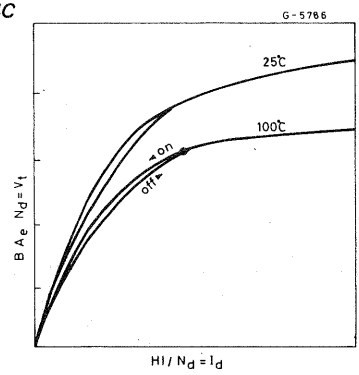
Winding I^2R losses are usually negligible. The drive transformer design in based on the following two considerations:

1. Magnetizing current I_{b1} is required for initial turn-on of the power switching transistor. During the time Q_2 is on, the magnetizing current will decrease due to voltage V_{be} across the base winding. The magnetizing current must not be allowed to decrease to less than zero, or it will cause premature turn-off under light load conditions by overcoming the small proportional drive current I_b. Referred to the primary, the drive winding inductance must be large enough to prevent I_{d1} (Equation 3) from reaching zero with voltage V_{be} (N_d/N_b) during the longest possible "on" time (usually half the switching period, 1/2f):

2. Under light load conditions, relatively little charge is required to turn-off Q_2. C_1 will then have substantial voltage remaining which will be applied to the drive winding during the remainder of the "off" period. This will cause the magnetizing current (and its associated energy storage) to become much larger than desired. The problem is solved by designing the drive winding to saturate at a current level slightly greater than the desired value of magnetizing current, I_{d1}. This will result in dumping any excess energy remaining in C_1 and establishing a consistent starting point on the B-H characteristic at the beginning of each "on" period.

Figure 4C shows the B-H characteristic of the core as seen from the drive winding. For the vertical axis, B times core area A_e and N_d equals $\int V_d\, dt$ (Faraday's Law). For the horizontal axis, H times effective core length, ℓ, and divided by N_d equals the magnetizing current I_d, (Ampere's Law). The characteristic slope equals the drive winding inductance, L_d, and the area to the left equals the energy stored.

Fig. 4C



The operating point shown will satisfy the two requirements above if it exceeds I_{d1} on the horizontal axis and if it exceeds V_{be} $(N_d/N_b)/2f$ on the vertical axis under worst case conditions at high temperature. Procedually, use Faraday's Law with B close to saturation at high temperature and with the area, A_e, of the core selected. Solve for N_d:

$$\frac{V_{be}\,(N_d/N_b)}{2f} = B\, A_e\, N_d \quad (8)$$

Use the samllest permissible N_d equal to or greater than the value calculated above. An N_d value larger than the calculated amount simply means that the change in flux density will be less than the maximum permitted.

Next, use Ampere's Law with a value for H corresponding to the B value chosen before, the smallest permissible N_d from above, and I equal to I_{d1}. Solve for the magnetic path lenght, ℓ.

$$N_d\, I_{d1} = H\ell \quad (9)$$

Compare the actual ℓ_e value for the core selected with the value calculated above. If the actual ℓ_e of the core, is significantly larger than the calculated ℓ, it will be necessary to use either a smaller core, or use a larger permissible number of turns, N_d. Otherwise, the operating point will not be close enough to saturation, and the B and H levels will both be too low to prevent the magnetizing current from becoming negative at the end of the "off" period.

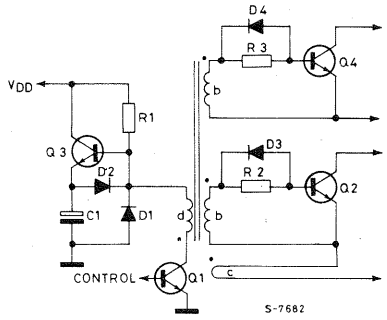
If the actual core ℓ_e is smaller than the calculated ℓ, the core will be too heavily saturated, and will not store enough energy to provide the desired I_{b1}. Either go to a larger core, or introduce a small gap, ℓ_g, according to the relationship:

$$\ell = (\ell_e + \mu_a \ell_g), \quad \text{where } \mu_a = B/H \qquad (10)$$

Driving Two Transistors. Two power switching transistors are often used in series in order to halve their high voltage V_{ce} rating requirements. It is usually desirable to drive these two transistors from a single drive circuit. This can be accomplished by means of two identical base windings in the transformer. N_b/N_c must be halved and N_d/N_b doubled from the values calculated in Eq. (1) and (2) because the total base current is twice as much as with a single transistor.

As shown in Figure 5C it is also necessary to add a small amount of resistance in series with each base in order to ensure current sharing. A resistor which drops 0.5V at maximum sustaining base drive, I_b, should be adequate. The added resistance does not affect the calculation of N_d in Equation (8) because its voltage drop is negligible compared to V_{be} under light load conditions, when the sustaining base drive is small. However, during turn-off, each series base resistor must be shunted by a small diode. Otherwise, a very large V_{bb2} value would be required in order to pull the desired I_{b2} out of each base. The forward drop on this diode must be added to the V_{bb2} requirement in Eq. (2).

Fig. 5C - Two-transistor driver



Line-side vs. Output-side Control Circuit The base and collector windings of the drive transformer are normally on the input, or line side, of the power supply. When the control/driver circuits are located on the output side of the supply, high voltage insulation is required between the drive winding and the base and collector windings. This high voltage insulation, usually greater than 3000V, will impair the coupling between line-side and output-side windings. This results in high leakage inductance, causing voltage spikes during turn-on and turn-off which may necessitate additional snubbing or clamping the drive transistor collector and the power switching transistor base.

When the control and driver circuits are located on the line side, the drive transformer does not require high voltage insulation. Leakage reactance can be made almost negligible, especially if multifilar windings are employed.

References:

(1) J. Gregorich and W. Hazen, "Designing Switched-Mode Converters with a New Proportional Drive Technique," Proceedings of POWERCON 5, May 1978, pp. E2 (1-8).

(2) P. Wood, "High Efficiency, Cost Effective Off-line Switching Converters," TRW Applications Note 143, April 1978, pp. 3-4.

(3) R. Severns, "A New Improved and Simplified Proportional Base Drive Circuit" Proceedings of POWERCON 6, May 1979, pp. B2 (1-12).

THE UC1524A INTEGRATED PWM CONTROL CIRCUIT PROVIDES NEW PERFORMANCE LEVELS FOR AN OLD STANDARD

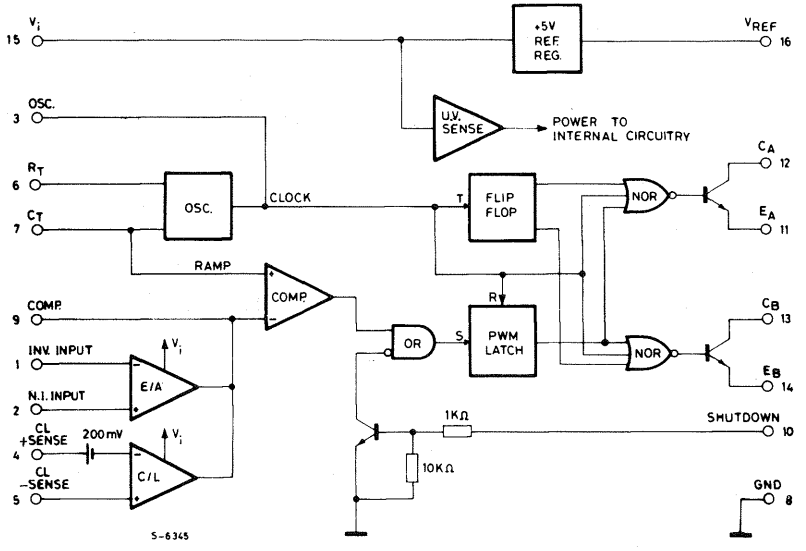
INTRODUCTION

The application of IC technology to the switching power supply really began with the introduction of the SG1524 in 1976. This device was the first IC to implement all the control blocks necessary for a wide range of PWM power systems. Its straight-forward approach to the classic PWM architecture gave it wide acceptance, and it has become the most commonly used IC controller today.

Even though the 1524 has gained great acceptance and engineers have praised its versatile and easy to understand architecture, they have many times cursed the simplistic, or idealistic, ways its individual blocks were implemented. While one would assume, at first glance, that all control functions necessary for most power supply applications are contained within the 1524, in the real word of practical power systems, additional circuitry is required to interface with the rest of the system, to protect against different types of fault conditions, to adjust for inaccuracies, or to improve control during power sequencing.

Although in the intervening years, many new IC control chips have been introduced which offer certain specialized advantages, it was found that

Fig. 1 - The UC1524A block diagram follows the same architecture as the SG1524 but with several significant differences.



design engineers still preferred the 1524 for its wide versatily and generalized architecture. From this understanding, it became apparent that a new design, which would improve many of the 1524's individual functions by making them more predictable and easier to apply, while retaining the same architecture, could be a winner. The result is the UC1524A.

THE UC1524A PWM CONTROLLER

A design goal set for the UC1524A was that it not only retain the same architecture but keep the same pin configuration as the 1524 and function equal to or better than the 1524 in most existing applications. In this way, engineers who were familiar with the 1524 could easily understand and evaluate the UC1524A. Performance improvements had to be significant, particularly in reducing the need for discrete support circuitry, so there would be cost advantage in using the UC1524A in new design. The block diagram of the UC1524A is shown in Figure 1 which, by intent, appears very similar to that of the older 1524.

The list of the improvements, however, is considerable and includes the following:

1. The 5V reference is now internally trimmed to ± 1% accuracy, eliminating the need for potentiometer adjustments.
2. The error amplifier's input range now extends beyond 5V, eliminating the need for a pair of dividers and their attendant tolerances.
3. A high-gain, wide-band, current sense amplifier has been included which is useful for either linear or pulse-by-pulse current limiting in the ground or power supply output lines.
4. An under-voltage lockout circuit has been added which disables all the internal circuitry except the reference until the input voltage has risen to 8V. This holds standby current low until turn-on, greatly simplifyng the design of low-power, off-line converters. There is approximately 600mV of hysteresis included for jitter-free activation.
5. A PWM latch has been added insuring freedom from multiple pulsing within a period, even in noisy environments. In addition, the shutdown circuit feeds direclty to this latch which will disable the outputs within 200ns of activation.
6. The oscillator circuit is usable to frequencies beyond 500KHz and is easier to synchronize with an external clock pulse.
7. The power capability of the output switches has been boosted by doubling the current capability to 200mA and increasing the voltage rating to 60V.

An understanding of some of these improvements is necessary for ease in application and will now be discussed in greater detail.

INTERNAL POWER TURN-ON CIRCUIT

The under-voltage lockout and turn-on hysteresis circuit is shown in Figure 2. This circuit requires approximately 2V for activation; but, since nothing else will turn on without at least 3V of supply voltage, lockout is assured. When V_i rises above 2V, R_2 begins to conduct saturating Q_3 and holding the base of Q_5 too low to allow any of the current sources to conduct. The current through R_4 flows through Q_3 and R_3, developing a 600mV drop across R_3 when V_{REF} reaches 5V. At this level, the only current flowing is that used by the reference regulator and R_2 and R_4, a total of approximately 2.5mA at turn-on threshold.

When the input voltage reaches approximately 8V, diode Z begins to conduct turning on Q_2 which turns off Q_3 and allows the current sources to activate. Since the current through Q_2 is much less than through Q_3, the voltage across R_3 drops, providing positive feedback. This gives about 600mV of hysteresis. This circuit, of course, works in reverse at turn off, insuring that the outputs can only operate when the supply is adequate for fully predictable operation. Figure 3 shows the relationship between quiescent current and input voltage. Designers should find this low current start-up characteristic quite advantageous for off-line, primary-side control with boot-strapped operation after turn on.

Fig. 2 — The under-voltage lockout and power turn-on circuitry within the UC1524A

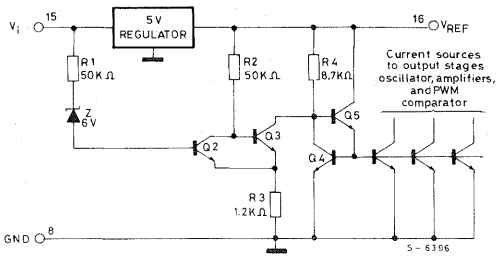


Fig. 3 - Supply current for the UC1524A vs. input voltage

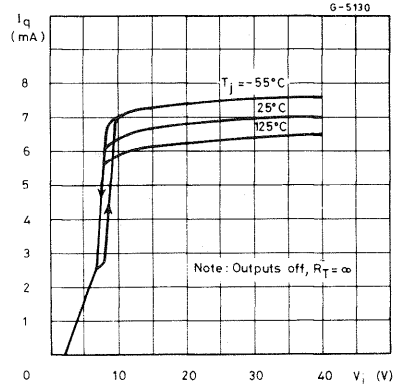
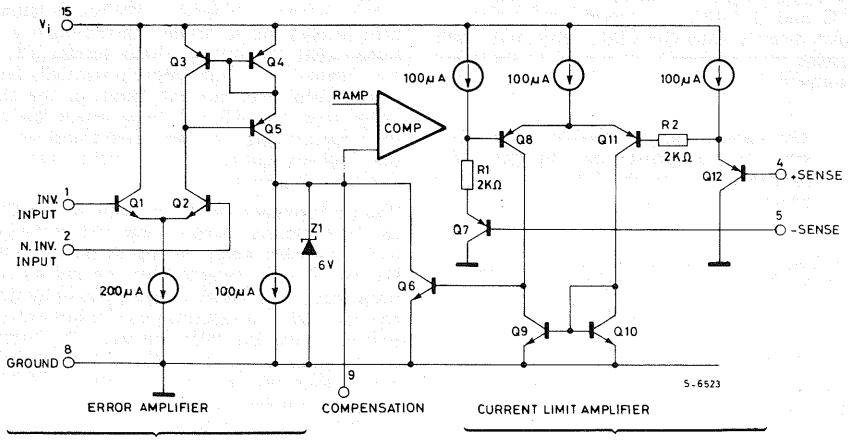


Fig. 4 - Voltage and current sensing amplifiers have a common output at the input to the PWM comparator.



A NEW CURRENT LIMIT AMPLIFIER

Since the outputs of the current limit amplifier and the voltage-sensing error amplifier are summed at the PWM comparator input, they should be examined together as shown in Figure 4.

Since the error amplifier, consisting of transistors Q_1 through Q_5 must have the lowest priority in controlling the PWM, its output must be easily overruled by current faults or other programming functions, such as soft-start, which would hold pin 9 low. Therefore, a transconductance amplifier similar to that used in the earlier 1524 was again applied to the 1524 with one exception: it is now powered by V_i instead of V_{REF}, so that the input common-mode range extends to within 2V of either rail. Zener diode, Z_1, is used on the output to keep the input level to the PWM comparator below 6 volts.

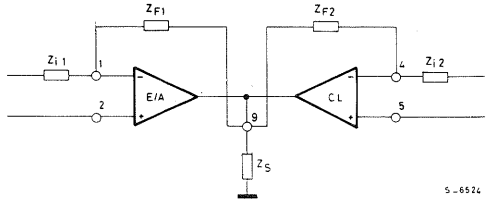
The error amplifier's output can be considered a 100μA current source or sink (0 - 200μA source with 100μA constant sink). When the current limit circuit activates, Q_6 turns on and can easily pull down pin 9 even though the error amplifier would nominally be calling for a high output at this point.

The current limit circuit consists of Q_6 through Q_{12}. Its differential PNP input stage gives it a common mode range extending from 300mV below ground to within -2V of V_i. Its threshold or offset, of 200mV is established by the 100μA current source through R_1, with R_2 added to null out the effect of any base current from Q_8.

This current sensing block within the UC1524A can actually be used either as a linear amplifier or as a comparator. The open loop small-signal gain is approximately 80dB while its transition delay with 10% overdrive is 600ns. This can be decreased substantially with additional overdrive. Use of the current sensing block as a comparator is usually preferred from a systems standpoint, since it does not have to be compensated and pin 9 can be dedicated solely to error amplifier compensation. Under this condition, a current signal over the threshold level will pull pin 9 low, terminating the output signal. Recovery is determined by the 100μA pull-up current from the error amplifier in conjunction with any capacitance which may be present on pin 9.

When the current limit circuit is used as a linear amplifier, stabilization is performed by feedback to the inverting input (pin 4) or by capacitance from pin 9 to ground as shown in Figure 5.

Fig. 5 - Various compensation options which are possible when both amplifiers are operated in the linear mode.

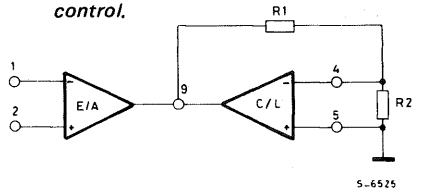


An additional feature of this circuit is its capability to perform as a duty-cycle limiting circuit in the configuration shown in Figure 6. If R_1 is made 100KΩ, there will be minimal effect upon the error amplifier gain.

In current limiting, to achieve the fastest responding pulse-by-pulse control, consideration should be given to the use of the shutdown terminal on pin

10. While the input threshold of this circuit is not as accurately controlled as the current limit amplifier and has a negative temperature coefficient of -2mV/°C and is internally ground referenced; it does feed directly into the PWM latch with only 200ns delay from activation of pin 10 to shutdown of the outputs.

Fig. 6 - The fixed 200mV threshold of the current limit amplifier can be multiplied to form a duty-cycle clamp or dead-band control.



Maximum duty cycle (%) $40\left[0.2\left(\frac{R1}{R2}+1\right)-1\right]$

PWM COMPARATOR AND LATCH

The PWM latch insures only a single pulse is allowed to reach the appropriate output stage within each period. The latch is reset with the oscillator clock pulse which also serves to black the outputs. Thus, although the latch is reset at the start of the oscillator clock pulse, it is the termination of the clock pulse which initiates output conduction. The output then stays on until the latch is set, either by a signal from the PWM comparator or from a shutdown command from pin 10. Once the latch is set, it will hold the output off for the duration of the period.

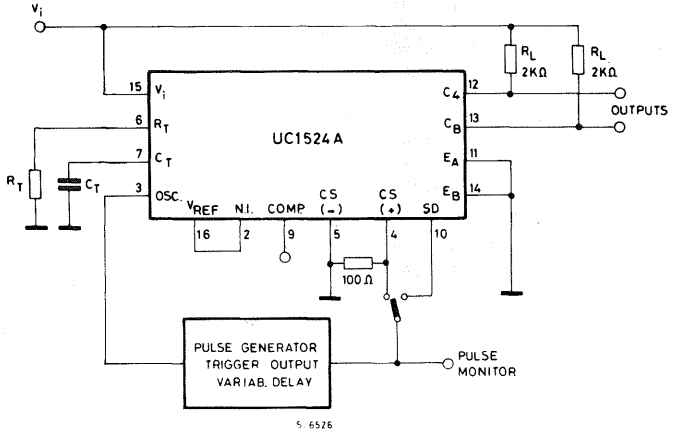
These are several significant advantages to this circuit. First, the latch completely elimitates multiple outputs of the PWM comparator because of noise or ringing on the output of the error amplifier causing multiple crossing of the ramp signal. Second, current limiting can now be performed much more rapidly without instability. Without a latch, significant integration is needed to maintain a turn-off signal after the outputs have turned off. Finally, any instabilities which might potentially be present in the voltage or current loops, or the shutdown signal from pin 10, will cause much less stress on the output stages, since only two transitions through the high-dissipation active region can be made during each period.

The performance or this portion of the UC1524A can be evaluated using a triggerable pulse generator with a variable delay, set up as shown in Figure 7. R_T and C_T are selected for the desired operating frequency. The clock triggers the pulse generator, and the delay is adjusted so the generator output occurs during the PWM period. The output pulse width must be at least 200ns and the amplitude higher than the threshold of the UC1524A input being evaluated. Typical waveform photographs are shown in Figure 8.

HIGHER POWER OUTPUT SWITCHES

With the higher current and voltage rating of the UC1524A's output switches, significant economies can now be achieved in interfacing with higher power devices. For low power requirements, a broader range of applications may now be served by the 1524A itself without additional discrete output devices. Regardless of the power supply requirement, more current and voltage from the UC1524A will ease the design tradeoffs. Even with higher current and voltage, the UC1524A offers fast response time. Each output stage contains an anti-saturation network to keep the output transistors out of hard saturation. Although this adds somewhat to the saturation voltage, it is more than offset by the benefits in reducing turn-off delay.

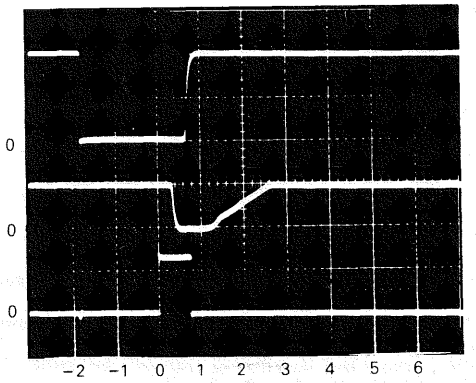
Fig. 7 - Evaluating the turn-off delays of the UC1524A with the aid of a triggerable pulse generator with variable delay.



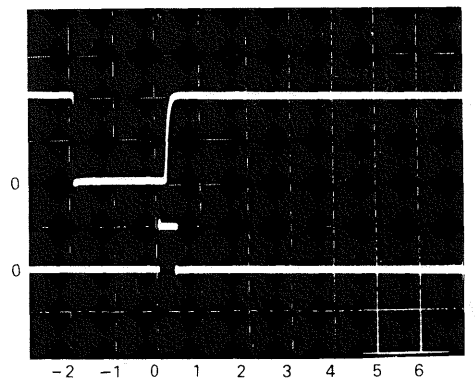
Saturation voltage as a function of current is shown in Figure 9.

Since both collectors and emitters are available on the UC1524A's output transistors, many different coupling possibilities are offered. One useful configuration for enhanced turn-off is shown in Figure 10. The fast-rising signal appearing at the collector of the output transistor, Q_1, is capacitively coupled to saturate an external transistor, Q_2, greatly reducing the turn-off delay of Q_3 and allowing a much larger value to be selected for R_3. Many variations of this circuit are possible depending upon the power devices to be driven and the voltage levels required.

Fig. 8 - Typical turn-off response from both the current sense and shutdown inputs.



Top — Output, 10V/div
Middle — Comp output, 5V/div
Lower — Current sense input, 200mV/div
Time — 1μs/div



Upper — Output, 10V/div
Lower — Shutdown input, 1V/div
Time — 1μs/div

Fig. 9 - Output saturation characteristics for each of the UC1524A's outputs.

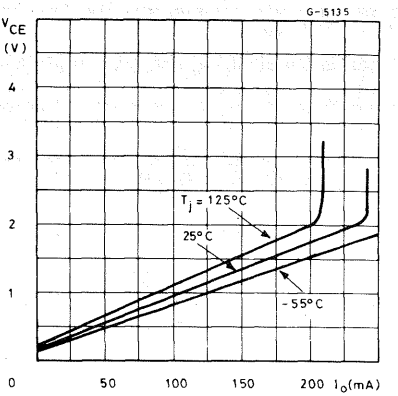
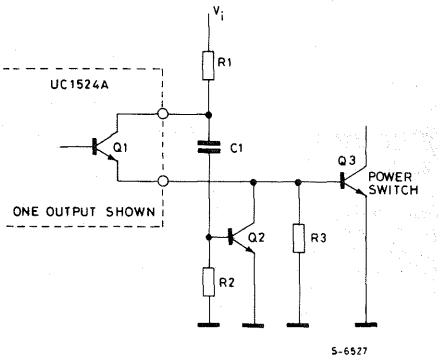


Fig. 10 - The addition of C_1 and Q_2 uses the collector signal of the UC1524A to generate an enhanced turn-off command for Q_3



FREQUENCY SYNCHRONIZATION

The oscillator circuit within the UC1524A, shown in Figure 11, has been improved over that of the 1524 with the addition of C_2. Without this component a synchronizing pulse externally applied to pin 3 had to do all the work of discharging the timing capacitor through Q_4 and Q_5. The simple addition of C_2 couples a positive pulse from pin 3 to the base of Q_{10}, momentarily reducing the threshold of comparator Q_8-Q_9 and regeneratively triggering the oscillator into its discharge state. The circuit is now leading-edge triggered and narrow pulses can be used. This is a consideration when minimum dead time is required, since the outputs are blanked off as long as pin 3 is held high.

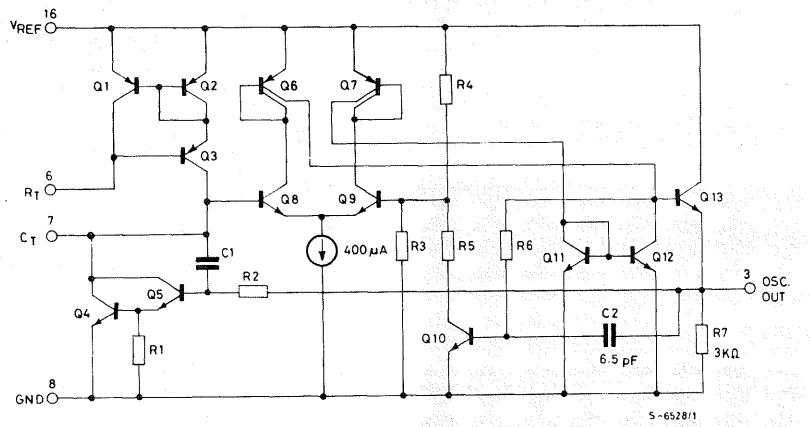
As with the 1524, synchronization to an external clock should be done with the R_T C_T time constant set approximately 10 to 20% greater than that determined for the required clock frequency, taking into consideration the expected tolerances of the

components. For synchronizing multiple UC1524A devices, all R_T, C_T, and OSC output terminals should be individually connected together and a single R_T and C_T used.

When considering blanking, the pulse on pin 3 may be extended somewhat by the addition of a capacitor of up to 100pF from pin 3 to ground. If narrower blanking pulses are required, adding a resistive load from pin 3 to ground of 1KΩ minimum will reduce the pulse width.

The best way to guarantee a large dead time is still to use a diode to clamp the peak output from the error amplifier to a divider from V_{REF}. This technique is quite accurate due to the accuracy of V_{REF} and the 100μA fixed current available from the amplifier.

Fig. 11 - The oscillator circuit of the UC1524A allows both high frequency operation and ease of external synchronization.



A COMPLETE DC-DC CONVERTER WITH THE UC1524A

An important attribute of the new UC1524A family is the higher voltage rating on the output transistors. This now makes it possible to implement a practical 4W DC-DC converter operating from a common 28V bus with no additional output transistors. The schematic of Figure 12 uses a push-pull configuration which imposes a voltage of twice the supply across the "OFF" transistor. This is now within the rating of the UC1524A and, thus, with a 28 : 7 turns ratio in the transformer, a 5V, ¾A output is achieved with 78% efficiency at a significant minimum parts count.

The fast response of the current limit amplifier within the UC1524A again keeps the device well protected as shown in the waveforms of Figure 13.

Fig. 12 - With higher output voltage capability, the UC1524A can implement a complete 4W DC to DC converter with no additional switching transistors.

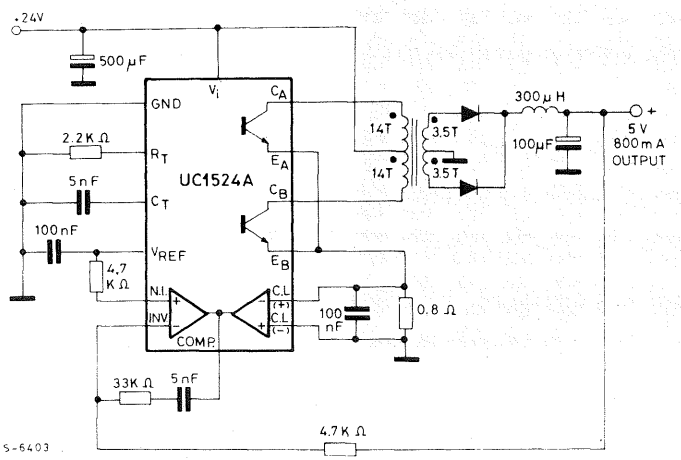
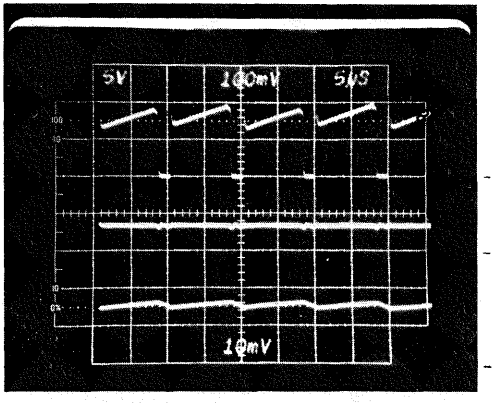
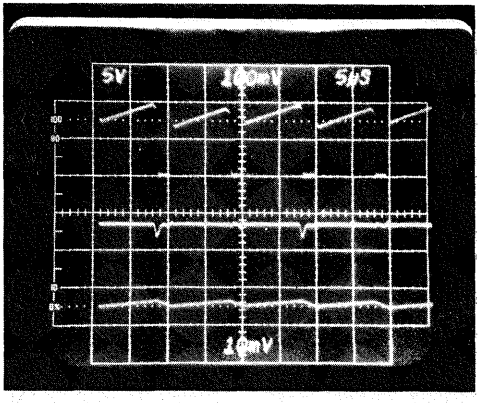


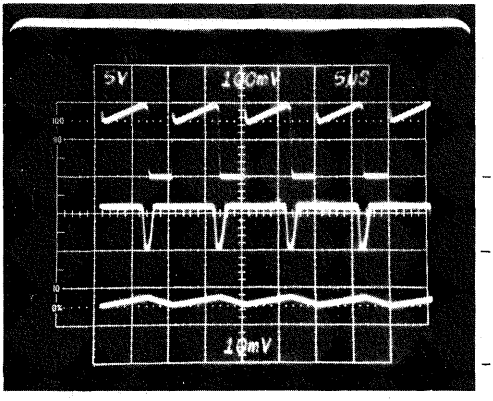
Fig. 13 - Operating waveforms for the PWM DC-DC converter (Fig. 12)
Upper trace = Primary current at 0.1A/division
Middle trace = Pin 9 voltage at 5V/division
Lower trace = Load current at 0.5A/division
Time base = 5µs/division



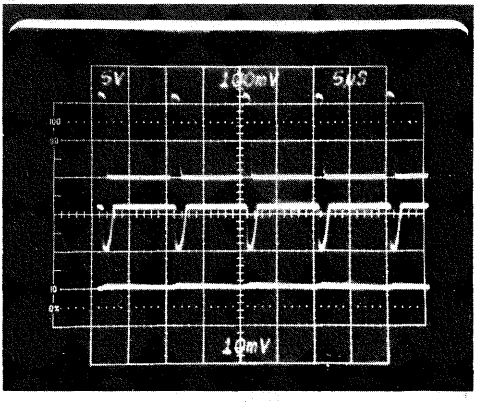
Circuit under normal load



Circuit at threshold of current limiting



Circuit under full current limit



Circuit under short circuit conditions

AN OFF-LINE FORWARD CONVERTER

For low to medium power application single-ended flyback or forward converter with all the control on the primary side of the isolation step-down transformer is usually the most economical solution. However there are two complications with this approach. The first is that although the control circuitry can easily be driven from a low-voltage winding on the power transformer, starting energy must be taken from the high-voltage rectified line where, at 170VDC, every 10mA represents a 1.7W loss. The second complication is in obtaining adequate regulation of the output while still meeting isolation requirements from output back to the line.

The 50W forward converter of Figure 14 offers innovative solutions to both these problems. In this circuit, the UC1524A provides all the control with its operating drive power coming from winding N_2. The low-current start-up characteristics of the UC1524A allow starting energy to be developed in C_2 with only approximately 8mA required through R_1.

The problem of isolated feedback control is solved in this application by sampling the 5V output level at the switching frequency be means of the 2N2222 transistors and transformer T_2. With every switching cycle, the output voltage is transferred from N_1 to N_2 where it is peak detected to generate a primary-referenced signal to drive the PWM

Fig. 14 - This 50W off-line forward converter features both high efficiency and good regulation while maintaining input-output isolation.

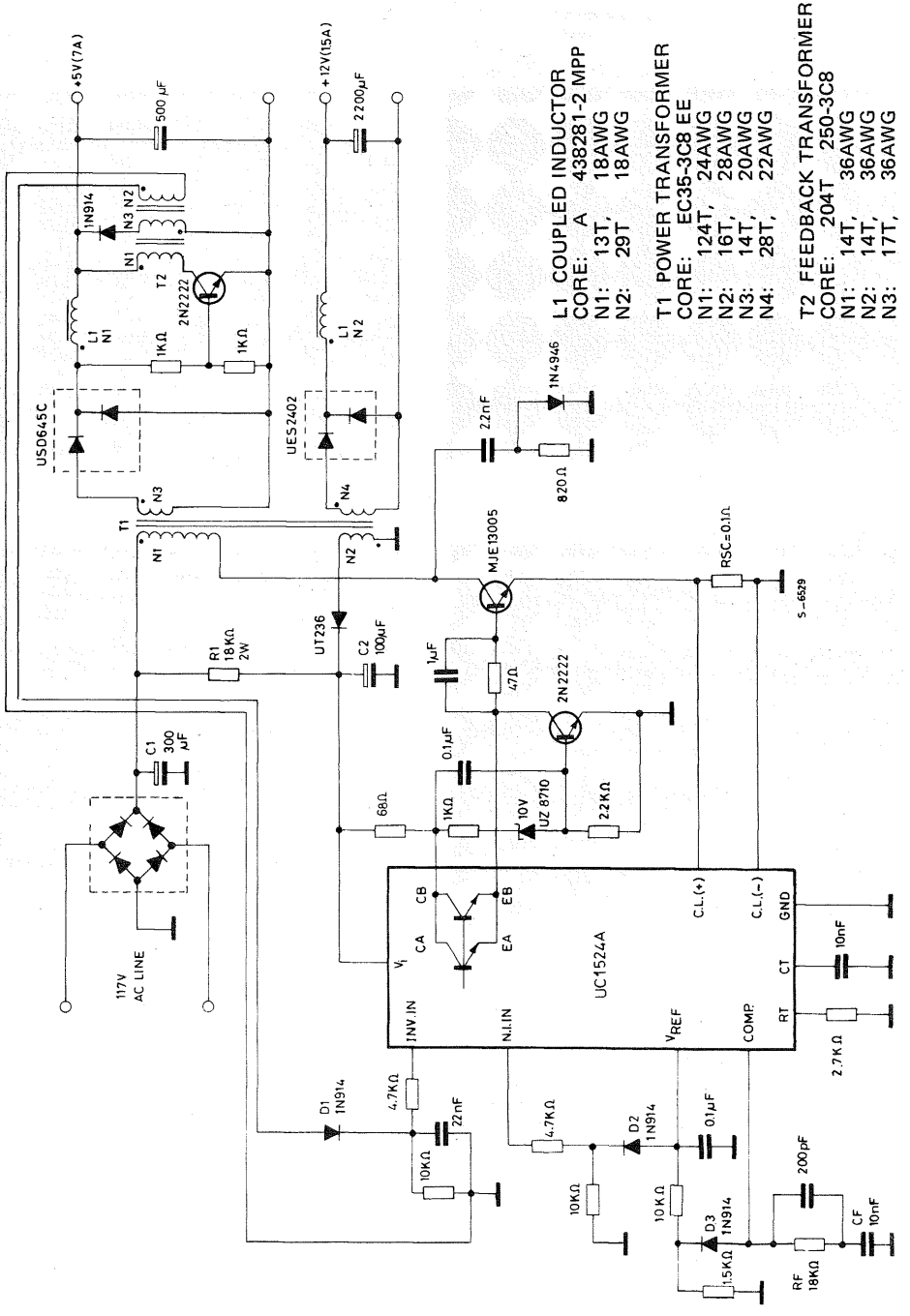
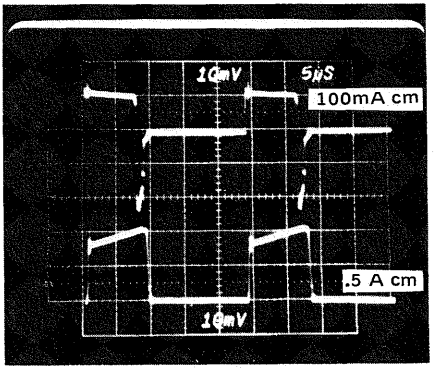


Fig. 15 - Base current (upper trace) and collector current for the MJE13005 of fig. 14. The time base is 5μs per division



at Full Load (50W)

error amplifier. Diode D_2 is used to temperature compensate for the loss in the rectifier, D_1 and the net result is better than 1% regulation with the main added cost that of a very inexpensive signal transformer.

Some of the other features of this application include a duty-cycle clamp on the PWM formed by diode D_3 and the 10K - 1.5K divider from V_{REF}. This method of clamping is more effective with the UC1524A since the UV lockout keeps the outputs off until the reference, error amplifier, and oscillator are all operating within specification.

Drive for the MJE13005 high-voltage switch is accomplished by using the emitters of the UC1524A's output transistors for turn-on and the 2N2222 in conjunction with the 1μfd base capacitor to provide a negative base voltage for rapid turn-off as described in Figure 10.

The resultant drive signal is shown in Figure 15. Operating at 40KHz, this regulator provides an isolated 50W of power with an efficiency of 83% , a high degree of regulation, and fast overload protection.

CONCLUSION

Although there are now many new integrated circuits from which to choose in attempting to build more cost-effective power supplies, it always helps to review well established ideas. In the case of the UC1524A, updating and improving an earlier product has resulted in a significant advancement providing greater performance and versatility while reducing system costs.

A SECOND-GENERATION IC SWITCH MODE CONTROLLER OPTIMIZED FOR HIGH FREQUENCY POWER MOS DRIVE

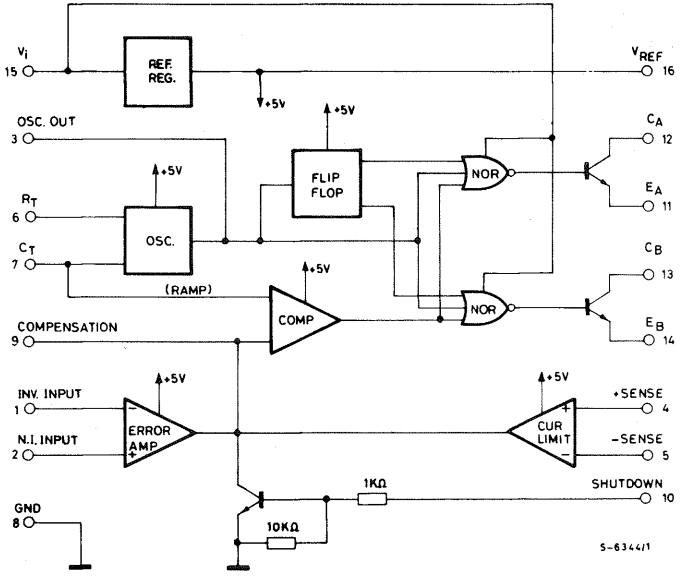
INTRODUCTION

Since the introduction of the SG1524 in 1976, integrated circuit controllers have played an important role in the rapid development and exploitation of high-efficiency switching power supply technology. The 1524 soon became an industry standard and was widely second-sourced.
Although this device contained all the basic control elements required for switching regulator design, practical power supplies still required other functions which had to be implemented with additional external discrete circuitry.

An additional development within the semiconductor industry was the introduction of practical Power Mos which offered the potential of higher efficiencies at higher speeds with resultant lower overall system costs.
In order to be able to take full advantage of the speed capabilities of power MOS, it was necessary to provide high peak currents to the gate during turn-on and turn-off to quickly charge and discharge the gate capacitances of 800 to 2000pF present in higher current units.

The development of a second-generation regulating PWM IC, the SG1525A, and its complimentary output version, the SG1527A, was a direct result of the desire to add more power supply elements to the control IC, as well as to optimize the interfacing of high current power devices.

Fig. 1 – The SG1524 regulating PWM block diagram.
This design was the first complete I.C. control chip for switch mode power supplies.

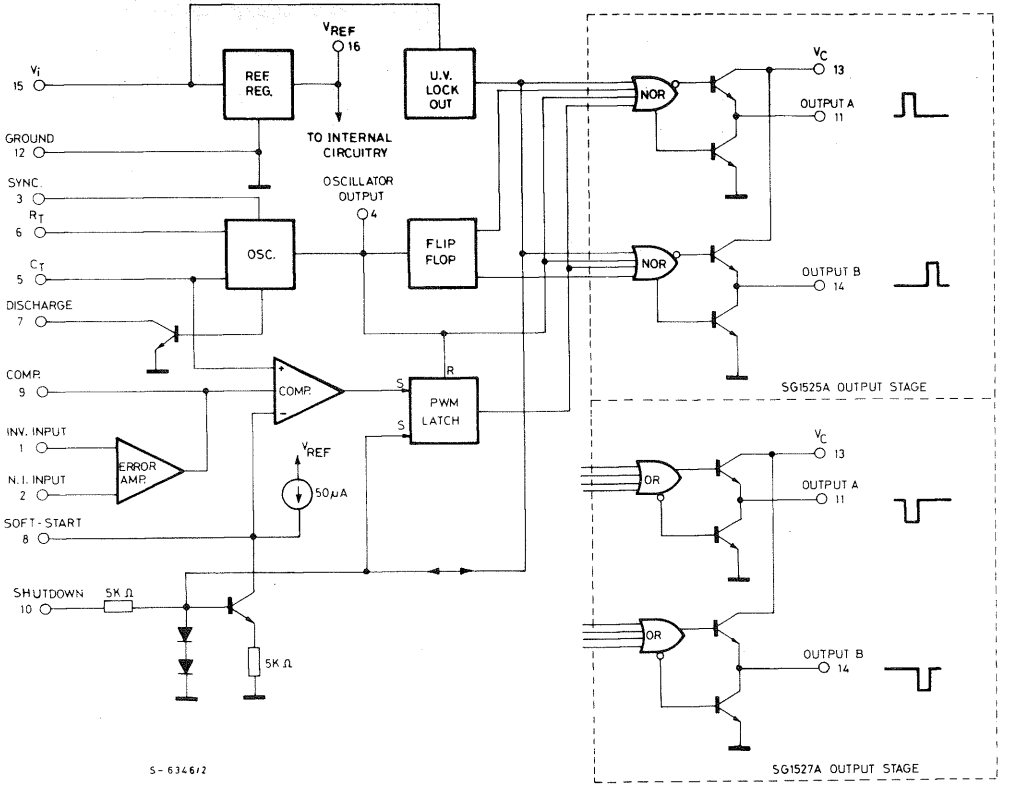


INTEGRATING MORE POWER SUPPLY FUNCTIONS

Having achieved the greatest level of acceptance among users of first generation control chips, the 1524 became the starting point for expanding IC controller capabilities. This early device, shown in Figure 1, contains a fixed-voltage reference source, an oscillator which generates both a clock signal and a linear ramp waveform, a PWM comparator, and a toggle flip-flop with output gating to switch the PWM signal alternately between the two outputs.

With this circuitry already defined, a two pronged development effort was initiated: 1) to add additional features required by most power supply designs and 2) to improve the utility of features already included within the 1524. The resultant block diagram for the SG1525A is shown in Figure 2. Two general comments should be made relative to the overall block diagram. First, in optimizing the output stage for bi-directional, low impedance switching, commitments had to be made as to whether the output should be high or low during the active, or ON state. Since this is application defined there are needs for both output states, so both were developed with the SG1525A device defined by an output configuration which is high during the ON pulse, and the SG1527A configured to remain high during the OFF state. This difference is implemented by a mask option which eliminates inverter Q_4 (see Figure 3) for the SG1527A. In all other respects, the 1525A and 1527A are identical and any description of the 1525A characteristics apply equally to the 1527A. Second, a major difference between this new controller and the earlier 1524 is the deletion of the current limit amplifier. There are so many system considerations in providing current control that it is preferable to leave this as a user-defined external option and allocate the package pins to other, more universally requested functions. Current limiting possibilities are discussed further under shutdown options.

Fig. 2 — The SG1525A family represents a "second generation" of IC controllers.

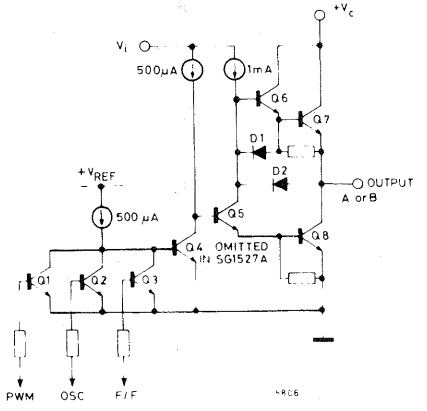


"TOTEM-POLE" OUTPUT STAGE

One of the most significant benefits in using the SG1525A is its output configuration. For the first time it has been recognized in an IC controller that it is more difficult to turn a power switch off than turn it on. With the SG1525A, a high-current, fast transition, low impedance drive is provided for both turn-on and turn-off of an external power transistor or Power MOS. The circuit schematic of one of the two output stages contained within the device is shown in Figure 3. This is a two-state output, either Q_8 is on, forming a low saturation voltage pull-down, or Q_7 is on, pulling the output up to V_C. Note that V_C is a separate terminal from the V_i supply to the rest of the device.

This offers the benefits of potentially operating the output drive from a lower supply than the rest of the circuit for power efficiencies, decoupling of drive transients from more sensitive circuits, and a third terminal for extracting a drive signal. Note that even though V_C can be set either higher or lower than V_i, the output cannot rise higher than approximately 1½ volts below V_i.

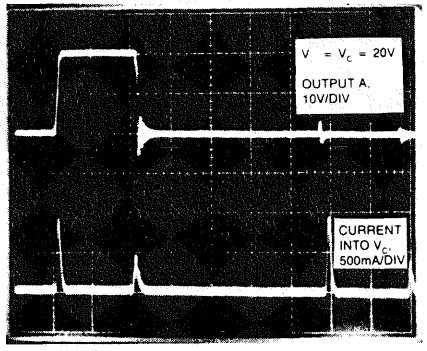
Fig. 3 – One of two power output stages contained within the SG1525A which conduct alternately due to the internal flip-flop.



During the transition between states, there is a slight conduction overlap between source and sink which results in a pulse of current flowing from V_C to ground. However, due to the high-speed design configuration of this stage, this current spike lasts for only about 100 ns. A typical current waveform at V_C is shown in Figure 4. This transient will normally be decoupled from the rest of the control power by a 0.1µF capacitor from V_C to ground but it should not, otherwise, cause a problem unless very high frequency operation is contemplated where it will contribute to overall device power dissipation, by becoming a significant portion of the total duty cycle.

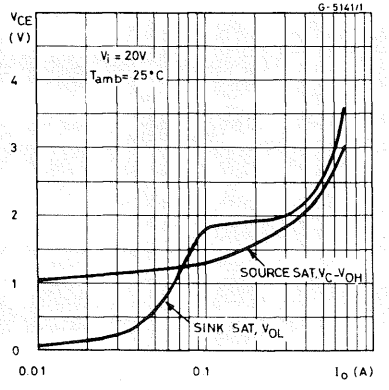
The output saturation characteristics of this stage are shown in Figure 5. The source transistor, Q_7 is a straight forward Darlington and its saturation voltage remains between 1 and 2V out to 400 mA under the assumption that $V_i \geq V_{CC}$. The sink transistor, Q_8, however, has a non-uniform characteristic which needs explanation. At low sink currents, the 1mA current source through Q_5 insures a very low saturation voltage at the output. As load current increases past 50 mA, Q_8 begins to come out of saturation for lack of base drive but only up to about 2V. Here diode D_2 becomes forward biased shunting a portion of the load current through Q_5 to boost the base current into Q_8. With this circuit, the sink transistor can both support high peak discharge currents from a capacitive load, as well as insure the low static hold-off voltage required for bipolar transistors.

Fig. 4 – Current "spiking" on the V_C terminal caused by conduction overlap between source and sink is minimized by high-speed design techniques.



HORIZONTAL = 500ns/DIV

Fig. 5 – The output saturation characteristics of the SG1525A provide both high drive current and low hold-off voltage.



A typical output configuration for a push-pull bipolar transistor power stage is shown in Fig. 6. With a steady state base drive current from the SG1525A of 100mA, this stage should be able to switch 1 to 5A of transformer primary current, depending

POWER SUPPLY SHUTDOWN

An important part of any PWM controller is the ability to shut it down at any time for a variety of reasons, including system sequencing requirements or fault protection. Several options are available to the user of the SG1525A, which require an understanding of the capability of the shutdown terminal, pin 10. Referring to Figure 11, the base of Q_5 is turned on by a signal which is clamped to approximately 1.4V by the action of D_1 and the V_{BE} of gates Q_3 and Q_4. This holds the outputs off and keeps C_{SS} discharged by Q_5 which, with R9, becomes a 100μA net current sink.

If, during normal operation, pin 10 is pulled high, three things happen. First, the outputs are turned off within 200ns through D_1. Second, the PWM latch is set by Q_6 so that even if the signal at pin 10 were to disappear, the outputs would stay off for the duration of that period, being reset by the next clock pulse. Third, Q_5 is activated commencing a 100μA discharge of C_{SS}. However, if the activation pulse on pin 10 has a duration shorter than $\frac{1}{3}$ of the clock period, the voltage on C_{SS} will remain high and soft-start will not be reactivated. Naturally, a fixed signal on pin 10 will eventually discharge C_{SS}, recycling soft-start.

Thus, the shutdown pin provides both sequencing capability as well as a convenient port for protective functions, including pulse-by-pulse current limiting.

REGULATING PWM PERFORMANCE IMPROVEMENTS

The SG1525A also offers significant performance and application improvements in almost all of the additional basic functions of a PWM over those obtainable with earlier devices. A general description of these features is outlined below:

Reference Regulator: The output voltage of this regulator is internally trimmed to 5.1V ± 1% during manufacture, eliminating the need for adjusting potentiometers in most applications.

Error Amplifier: SG1525A uses the same basic transconductance amplifier as the SG1524 with an important difference: it is powered by V_i rather than V_{REF}. Now the input common-mode range includes V_{REF} eliminating the need for a voltage divider with its attendant tolerances. An additional feature relative to the error amplifier is that the shutdown circuitry feeds into a separate input to the PWM comparator allowing pulse termination without affecting the output of the error amplifier which might have a slow recovery, depending upon the external compensation network selected. An important benefit of a transconductance amplifier is the ease with which its current mode output can be over-ridden by other external controlling signals.

PWM Comparator: The significant benefit of the SG1525A's PWM comparator is in its following latch. A common problem with earlier devices was that any noise or ringing on the output of the error amplifier would affect multiple crossings of the oscillator ramp signal resulting in multiple pulsing at the comparator's output. The SG1525A's latch terminates the output pulse with the first signal from the comparator, insuring that there can be only a single pulse per period, removing all jitter or threshold oscillation from the system. Another important advantage of this latch is the ability to easily implement digital or pulse-by-pulse current limiting by merely momentarily activating the shutdown circuitry within the SG1525A. This could be as simple as connecting pin 10 to a ground-referenced current sensing resistor. For greater accuracy, some added gain may be advantageous. Once a current signal causes shutdown, the output will remain terminated for the duration of the period, even though the current signal is now gone. An oscillator clock signal resets the latch to start each period anew.

Oscillator: The functions of the oscillator within the SG1525A have been broadened in two important aspects. One is the addition of a synchronization terminal, pin 3, allowing much easier interfacing to an external clock signal or to synchronize multiple SG1525A's together. The other is the separation of the oscillator's discharge network from its charging current source for deadtime control. Reference should be made to the schematic of Figure 12 for an understanding of the operation of this circuit. The heart of this oscillator is a double-threshold comparator, Q_7 and Q_8, which allows the timing capacitor to charge to an upper threshold by means of the current source defined by R_T and mirrored by Q_1 and Q_2. The comparator then switches to a lower threshold by turning on Q_{10} and discharges C_T through Q_3 and Q_4 with a rate defined by R_D. As long as C_T is discharging, the clock output is high, blanking the outputs.

Since the overall oscillator frequency is defined by the sum of the charge and discharge times, there are three elements now in the frequency equation which is approximately:

$$f \approx \frac{1}{C_T\,(.07\,R_T + 3\,R_D)}$$

External synchronization can easily be accomplished with a 2.8V positive pulse at pin 3. This will turn on Q_9, lowering the comparator threshold below wherever the voltage on C_T may happen to be. Two factors should be considered: First, the voltage on C_T determines the amplitude of the PWM ramp, and if the sync occurs too early, the loop gain will be higher and the resolution may be worse. Second, the sync circuit is regenerative within 200ns; and, while a wider pulse can be used, C_T will not begin to recharge as long as the sync pin is high. For synchronizing multiple SG1525A devices together, one need only to define a master with the correct R_TC_T time constant, connect its output pin to the slave sync pins, and set each slave R_TC_T for a time constant 10–20% longer than the master.

Fig. 12 – A simplified schematic of the SG1525A's oscillator circuitry.

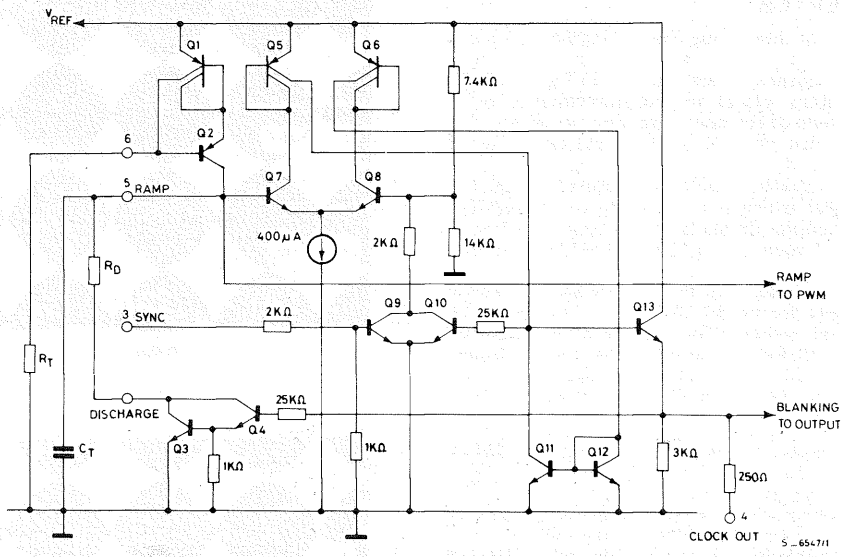
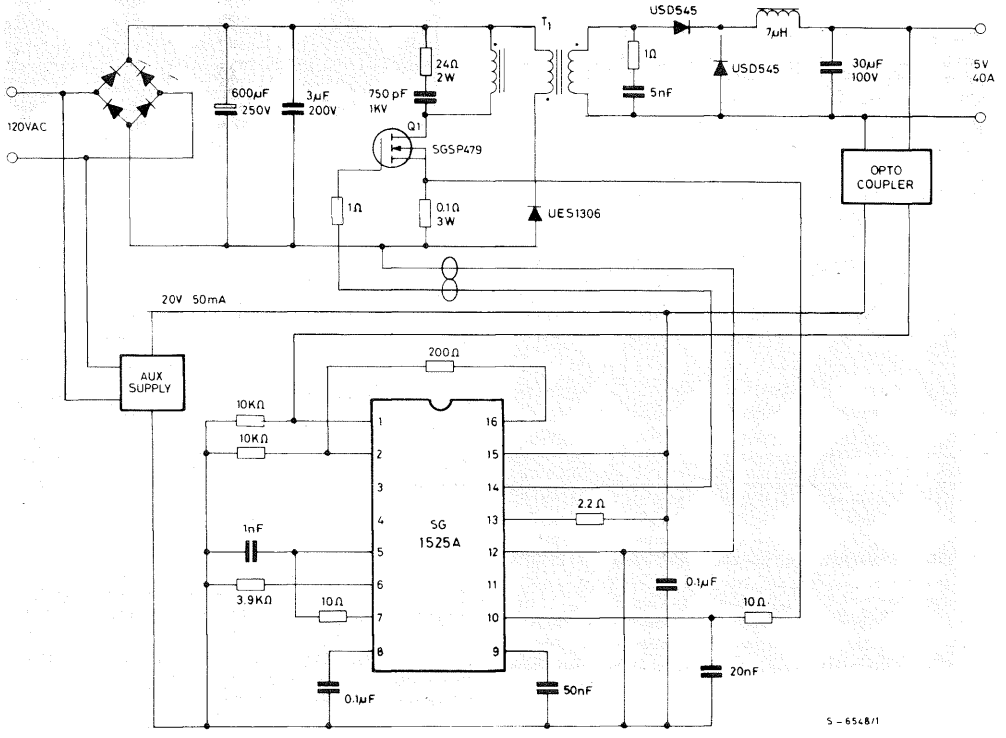


Fig. 13 – 200W, Off-Line Forward Converter.



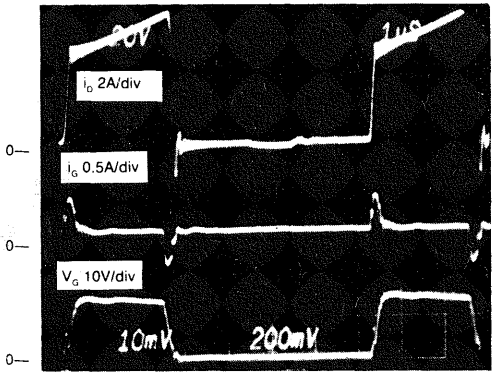
A 200 WATT, OFF-LINE, FORWARD CONVERTER

The ease of interfacing the SG1525A into a practical power supply system can be illustrated by the off-line, power converter shown in Figure 13. This 200W supply places the control circuitry on the primary side of the power transformer where direct coupling can be used to drive the power switch. While simplifying the drive electronics, this configuration usually requires an isolated voltage feedback signal which is most easily accomplished by an optocoupler driven by some type of voltage regulator IC such as a L123 or LM723. One other undefined block in Figure 13 is the auxiliary power supply which supplies the low voltage, low current bias supply for the SG1525A and the drive for Q_1, the power switch. The choice of the SGSP479 power MOS for this switch keeps the total power requirements from the auxiliary supply at less than 1W; readily implemented with a small, line-driven transformer.

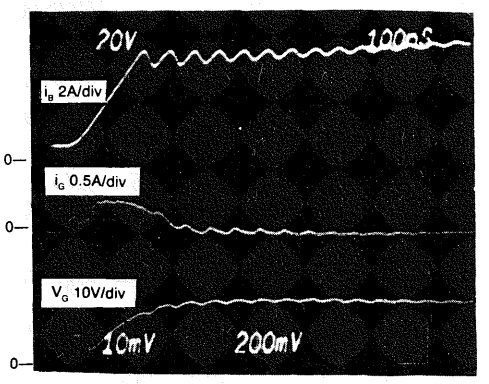
This converter is designed to operate at 150kHz which is accomplished by running the SG1525A at 300kHz and using only one of the outputs. This also automatically insures that the duty cycle can never be greater than 50%, a requirement of the power transformer in this configuration. The high operating frequency allows the output filter's roll-off to be set at 12kHz, greatly simplifying the overall loop stability considerations as adequate response can be achieved with only the single-pole compensation of the error amplifier provided by the 0.05μF capacitor on pin 9.

The totem-pole output of the SG1525A is used to advantage to drive Q_1 by providing a 400 mA peak current to charge and discharge the power MOS gate capacitance while keeping overall power dissipation low. Waveform photographs of this operation are shown in Figure 14.

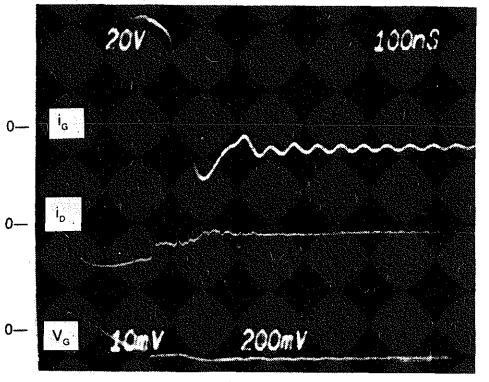
Fig. 14 – Current and voltage waveforms for the 200W off-line forward converter with a SG1525A direct driven power MOS switch (operating frequency is 150kHz with output current equal to 40A).



1μs/div
a) Waveforms of i_D, i_G, V_G



b) Risetime
≈ 90ns



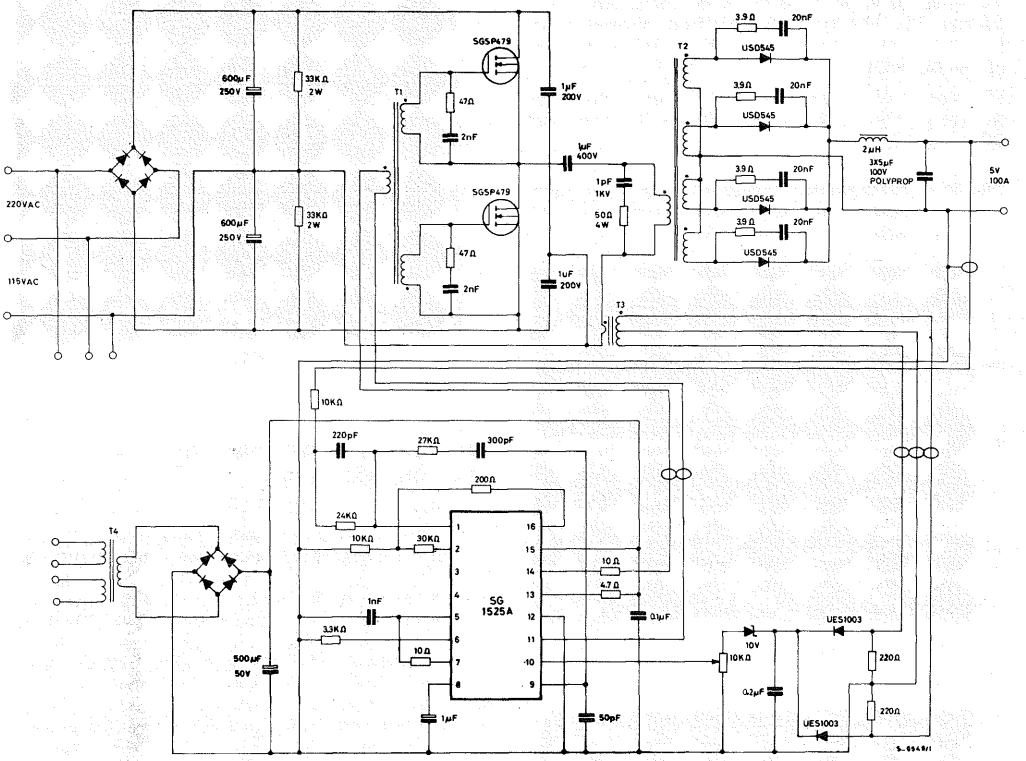
c) Falltime
≈ 30ns

When operating at full load, the efficiency of this converter is 73% with by far the greatest power losses occurring in the output rectifiers-even though Schottky devices have been selected.

Switching losses have been minimized by the fast current transitions, primarily defined by the leakage inductance of the transformer. Although this switching time could probably be even further reduced, there could be problems with current spikes during rise time due to Schottky rectifier capacitance.

Current limiting for this converter is provided by measuring the current in SGSP479 with the 0.1Ω resistor in series with the source and using this voltage to activate the shutdown circuitry within the SG1525A. While this will provide a fast-acting short circuit protection on a pulse-by-pulse basis, a comparator may need to be added for a more accurate current limit threshold.

Fig. 15 — 500W, 100 kHz Half-Bridge Schematic.



Transformer Winding Data

500W, 100kHz, Off-Line, Half-Bridge Converter:

T1 Core: Ferrox 486T250-3C8
Pri: 14T #22AWG
Sec (2): 7T #22AWG

T2 Core: Ferrox EC52-3C8 (EE)
Pri: 14T, 2 layers, 2 #16AWG in parallel
Sec (2): each 2T, C.T., copper strap 0.01" x 0.8"

T3 Core: Ferrox 486T250-3C8
Pri: 1T
Sec: 20T, C.T. #22AWG

T4 117V/220V, 25V, 0.15A, 50-60 Hz

L1 Core: Ferrox IF30-3C8
4 turns, 5 #12AWG in parallel

500 WATT, OFF-LINE, HALF-BRIDGE CONVERTER

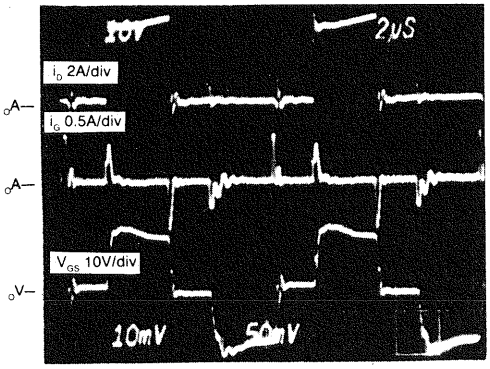
The circuit shown in Figure 15 uses a pair of SGSP479 power MOS in a half-bridge configuration with the SG1525A chip referenced to the secondary side of the power transformer.
The power MOS gates are driven directly from the control chip output through step down and isolation transformer T1. The SG1525A output terminals (pins 11 and 14) provide active pull-up and pull-down (dual source/sink) for the primary of T1. This provides the fast, high current turn-on and turn-off pulses needed for the power MOS gates. In addition, the two ends of the primary windings are shorted to ground during deadtime, which prevents accidental turn-on by transients. Note that the current supplied by the SG1525A outputs drops to a small value when the gate capacitance has been charged or discharged to the desired gate voltage. Damping resistors with series blocking capacitors across the two secondaries of T1 minimize ringing due to the power MOS gate capacitance and the inductance of T1 and lead inductance, particularly during deadtime.

Deadtime for the SG1525A is set very simply by a single resistor between pins 5 and 7. Only a small amount of deadtime is needed since the power MOS have no storage time and a very short delay time.
Slow turn-on is accomplished by a single capacitor at pin 8.

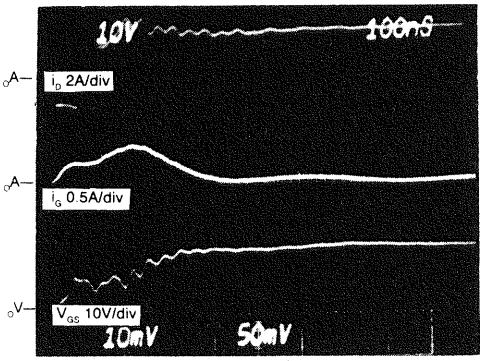
Current limiting is provided by current transformer T3 in series with the primary of the power transformer T2. The signal is rectified, threshold adjusted and sent to the shutdown terminal, pin 10, of the SG 1525A.

Waveforms of the converter are shown in the scope photos of Figure 16. Current rise and fall times are 20ns and 10ns.

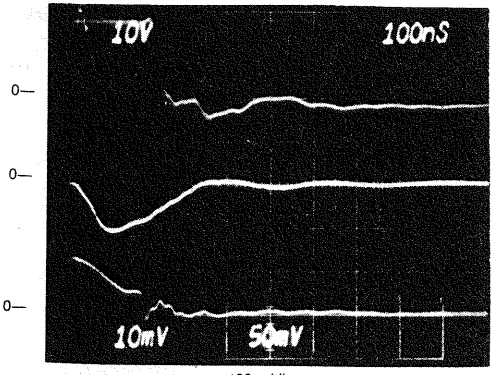
Fig. 16 – Performance waveforms for the half-bridge, 500W, 100kHz converter with output current of 80A.



2μs/div
a) Waveforms of i_D, i_G, V_G



100ns/div
b) Risetime



100ns/div
c) Falltime

IMPROVED PERFORMANCE; LESS COMPLEXITY

Although power supply designers for some time now have had an ever widening inventory of IC components available to ease their design tasks, the final measure of improvement has to be in terms of system performance versus cost. With fewer interface components to the power stages, freedom from potentiometer adjustments, protected start-up and shut-down, a built in soft-start network and several additional system-level features, the SG1525A provides a significant contribution to both performance and costs while simultaneously making the designer's task easier. With these accomplishments, it is clear that this device truly does represent a step-function improvement, introducing a second-generation of power control components.

A 25 WATT OFF-LINE FLYBACK SWITCHING REGULATOR

INTRODUCTION

This note describes a low cost switching power supply for applications requiring multiple output voltages, e.g. personal computers, instruments, etc. . . The discontinuous mode flyback regulator used in this application provides good voltage tracking between outputs, which allows the use of primary side voltage sensing. This sensing technique reduces costs by eliminating the need for an isolated secondary feedback loop.

The low cost, (8 pin) UC1842 current mode control chip employed in this power supply provides performance advantages such as:

1) Fast transient response
2) Pulse by pulse current limiting
3) Stable operation

To simplify drive circuit requirements, a TO-220 power MOS SGSP369 is utilized for the power switch. This switch is driven directly from the output of the control chip.

Power Supply Specifications

1. Input voltage: 95VAC to 130VAC (50Hz/60Hz)
2. Output voltage:
   - A. +5V, ± 5%: 1A to 4A load
     Ripple voltage: 50mV P-P Max
   - B. +12V, ± 3%: 0.1A to 0.3A load
     Ripple voltage: 100mV P-P Max
   - C. -12V, ± 3%: 0.1A to 0.3A load
     Ripple voltage: 100mV P-P Max.
3. Line Isolation: 3750V
4. Switching Frequency: 40KHz
5. Efficiency @ Full Load: 70%

Basic Circuit Operation

The 117VAC input line voltage is rectified and smoothed to provide DC operating voltage for the circuit. When power is initially applied to the circuit, capacitor C2 charges through R2. When the voltage across C2 reaches a level of 16V the output of IC1 is enabled, turning on power MOS Q1.

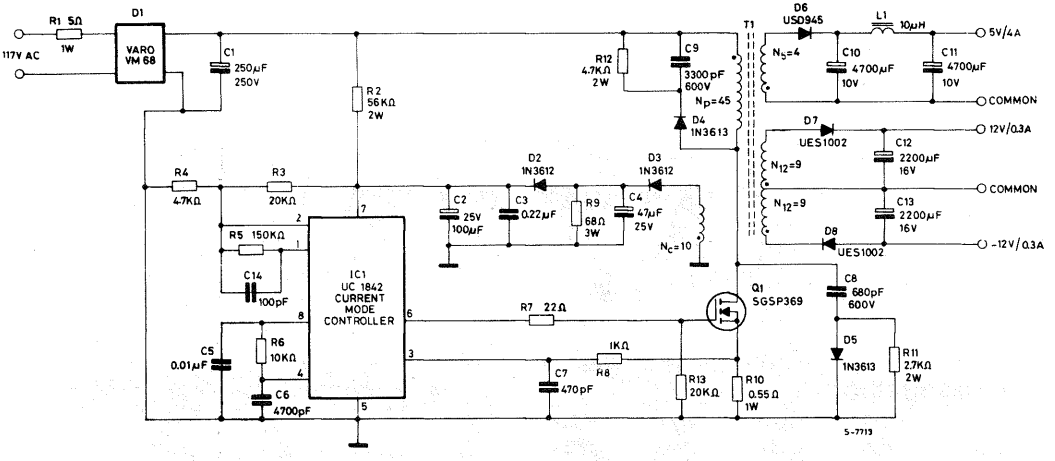
During the on time of Q1, energy is stored in the air gap of transformer (inductor) T1. At this time the polarity of the output windings is such that all output rectifiers are reverse biased and no energy is transferred. Primary current is sensed by a resistor, R10, and compared to a fixed 1V reference inside IC1. When this level is reached, Q1 is turned off and the polarity of all transformer windings reverses, forward biasing the output rectifiers. All the energy stored is now transferred to the output capacitors. Many cycles of this store/release action are needed to charge the outputs to their respective voltages. Note that C2 must have enough energy stored initially to keep the control circuitry operating until C4 is charged to a level of approximately 13V. The voltage across C4 is fed through a voltage divider to the error amplifier (pin 2) and compared to an internal 2.5V reference.

Energy stored in the leakage inductance of T1 causes a voltage spike which will be added to the normal reset voltage across T1 when Q1 turns off. The clamp consisting of D4, C9 and R12 limits this voltage excursion from exceeding the BVDSS rating of Q1. In addition, a turn-off snubber made up of D5, C8 and R11 keeps power dissipation in Q1 low by delaying the voltage rise until drain current has decreased from its peak value. This snubber also damps out any ringing which may occur due to parasitics.

Less than 3.5% line and load regulation is achieved by loading the output of the control winding Nc, with R9. This resistor dissipates the leakage energy associated with this winding. Note that R9 must be isolated from R2 with diode D2, otherwise C2 could not charge to the 16V necessary for initial start-up.

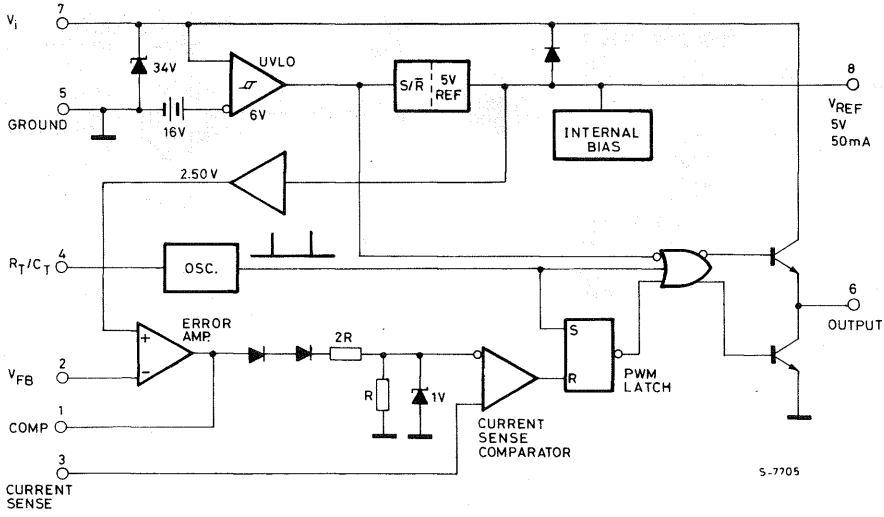
A small filter inductor in the 5V secondary is added to reduce output ripple voltage to less than 50mV. This inductor also attenuates any high frequency noise.

Fig. 1 - 25W off-line flyback regulator



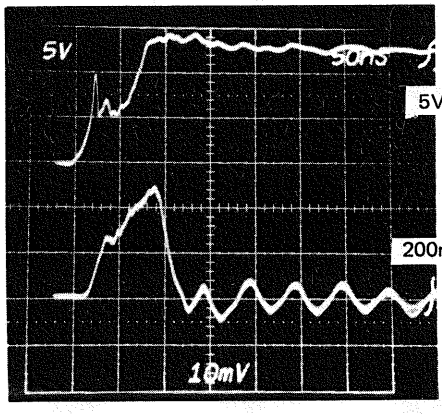
Notes 1 - All resistors are 1/4W unless noted
2 - See appendix for construction details
3 - L1 = Ferroxcube 204T50-3C8 (Toroid), N° turns: 4, Wire Gauge: 1mm. (18AWG)

Fig. 2 - Block diagram: UC1842 current mode controller

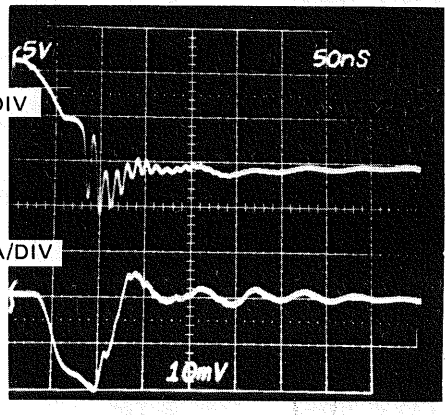


TYPICAL SWITCHING WAVEFORMS

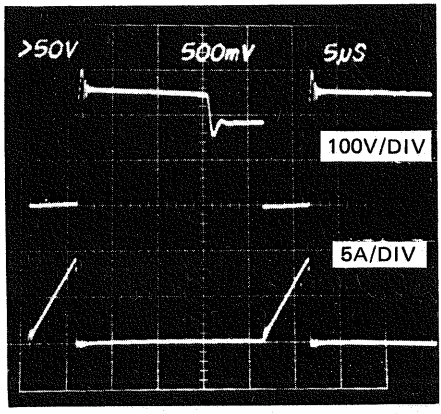
T_{on} – Drive waveforms



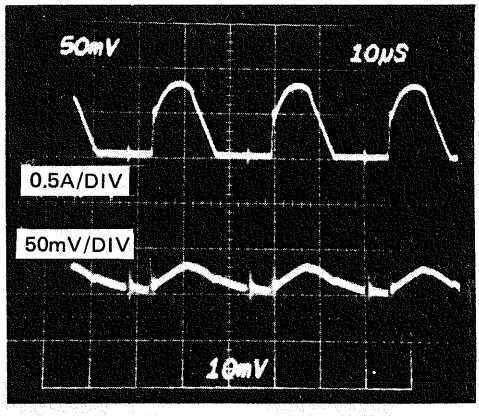
T_{off} – Drive waveforms



Upper trace: Q_1 – Gate to source voltage
Lower trace: Q_1 – Gate current



Upper trace: Q_1 – Drain to source voltage
Lower trace: Primary current – I_D



Upper trace: +5V charging current
Lower trace: +5V output ripple voltage

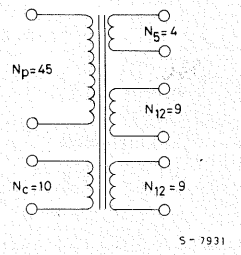
PERFORMANCE DATA

CONDITIONS		5V out	12V out	-12V out
Low Line (95VAC)				
± 12 @ 100mA	+5V @ 1.0A	5.211	12.05	-12.01
	4.0A	4.854	12.19	-12.14
± 12 @ 300mA	+5V @ 1.0A	5.199	11.73	-11.69
	4.0A	4.950	11.68	-11.63
Nominal Line (120VAC)				
± 12 @ 100mA	+5V @ 1.0A	5.220	12.07	-12.03
	4.0A	4.875	12.23	-12.18
± 12 @ 300mA	+5V @ 1.0A	5.208	11.73	-11.68
	4.0A	4.906	11.67	-11.62
High Line (130VAC)				
± 12 @ 100mA	+5V @ 1.0A	5.207	12.06	-12.02
	4.0A	4.855	12.21	-12.15
± 12V @ 300mA	+5V @ 1.0A	5.200	11.71	-11.67
	4.0A	4.902	11.66	11.61
Overall Line and Load Regulation		± 3.5%	± 2.3%	± 2.4%

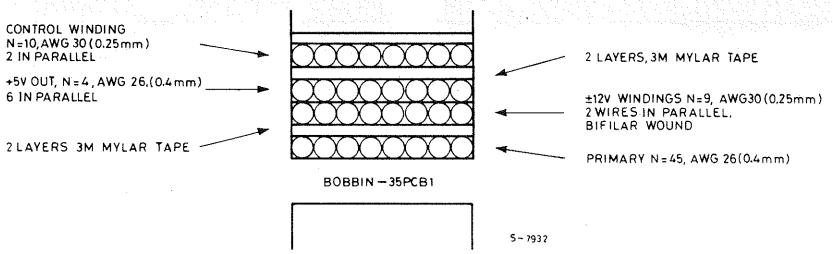
APPENDIX POWER TRANSFORMER -T1

Core: Ferroxcube EC-35/3C8
Gap: 0.25mm. in each outer leg

NOTE: For reduced EMI put gap in center leg only.
Use 0.5mm.



TRANSFORMER CONSTRUCTION



UC3842 PROVIDES LOW-COST CURRENT-MODE CONTROL

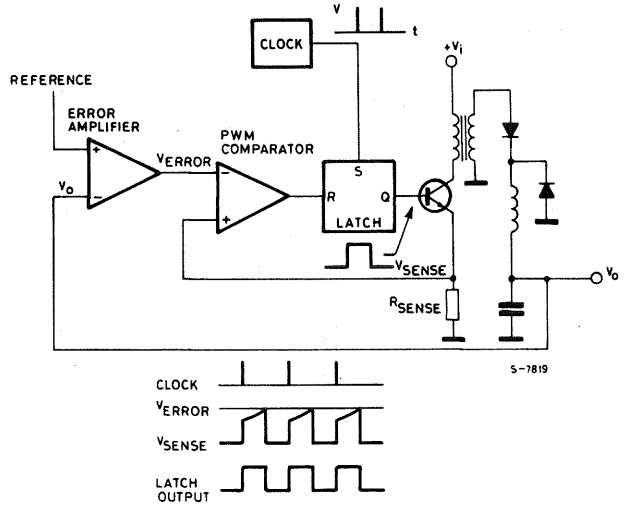
The fundamental challenge of power supply design is to simultaneously realize two conflicting objectives: good electrical performance and low cost. The UC3842 is an integrated pulse width modulator (PWM) designed with both these objectives in mind. This IC provides designers an inexpensive controller with which they can obtain all the performance advantages of current-mode operation. In addition, the UC3842 is optimized for efficient power sequencing of off-line converters and for driving increasingly popular POWERMOS.

This application note gives a functional description of the UC3842 and suggests how to incorporate the IC into practical power supplies. A review of current-mode control and its benefits is included and methods of avoiding common pitfalls discussed. The final section presents designs of two power supplies utilizing UC3842 control.

CURRENT-MODE CONTROL

Figure 1 shows the two-loop current-mode control system in a typical buck regulator application. A clock signal initiates power pulses at a fixed frequency. The termination of each pulse occurs when an analog of the inductor current reaches a threshold established by the error signal. In this way the error signal actually controls peak inductor current. This contrasts with conventional schemes in which the error signal directly controls pulse width without regard to inductor current.

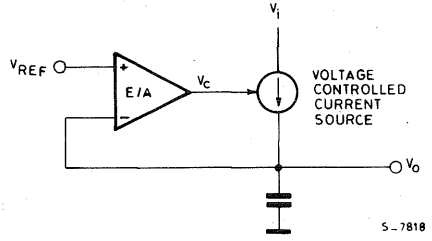
Fig. 1 – Two-loop current-mode control system



Several performance advantages result from the use of current-mode control. First, an input voltage feed-forward characteristic is achieved; i.e., the control circuit instantaneously corrects for input voltage variations without using up any of the error amplifier's dynamic range. Therefore, line regulation is excellent and the error amplifier can be dedicated to correcting for load variations exclusively.

For converters in which inductor current is continuous, controlling peak current is nearly equivalent to controlling average current. Therefore, when such converters employ current-mode control, the inductor can be treated as an error-voltage-controlled-current-source for the purposes of small-signal analysis. This is illustrated by Figure 2. The two-pole control-to-output frequency response of these converters is reduced to a single pole (filter capacitor in parallel with load) response.

Fig. 2 - Inductor looks like a current source to small signals



One result is that the error amplifier compensation can be designed to yield a stable closed-loop converter response with greater gain-bandwidth than would be possible with pulse-width control, giving the supply improved small-signal dynamic response to changing loads. A second result is that the error amplifier compensation circuit becomes simpler and better behaved, as illustrated in Figure 3. Capacitor C_i and resistor R_{iz} in Figure 3a add a low frequency zero which cancels one of the two control-to-output poles of non-current-mode converters. For large-signal load changes, in which converter response is limited by inductor slew rate, the error amplifier will saturate while the inductor is catching up with the load. During this time, C_i will charge to an abnormal level. When the inductor current reaches its required level, the voltage on C_i causes a corresponding error in supply output voltage. The recovery time is R_{iz} C_i, which may be milleseconds. However, the compensation network of Figure 3b can be used where current-mode control has eliminated the inductor pole. Large-signal dynamic response is then greatly improved due to the absence of C_i.

Fig. 3 - Required error amplifier compensation for continuos inductor current designs using (a) Dyty-cycle control and (b) Current-mode control.

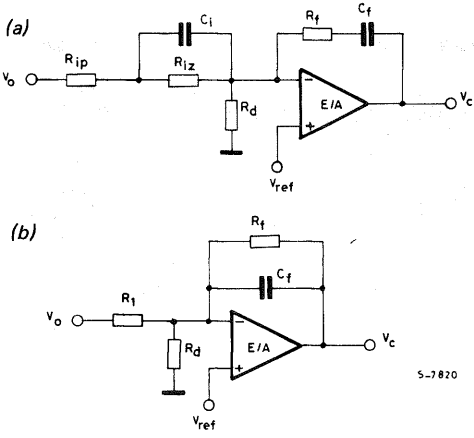
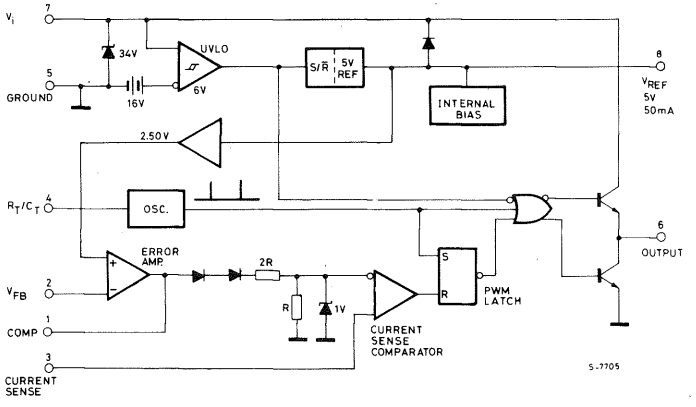


Fig. 4 - UC3842 block diagram



Current limiting is simplified with current-mode control. Pulse-by-pulse limiting is, of course, inherent in the control scheme. Furthermore, an upper limit on the peak current can be established by simply clamping the error voltage. Accurate current limiting allows optimization of magnetic and power semiconductor elements while ensuring reliable supply operation.

Finally, current-mode controlled power stages can be operated in parallel with equal current sharing. This opens the possibility of a modular approach to power supply design.

FUNCTIONAL DESCRIPTION

A block diagram of the UC3842 appears in Figure 4. This IC will operate from a low impedance DC source of 10V to 30V. Operation between 10V and 16V requires a start-up bootstrap to a voltage greater than 16V in order to overcome the under-voltage lockout. V_{CC} is internally clamped to 34V for operation from higher voltage current-limited sources ($I_{CC} \leqslant 30mA$).

Under-Voltage Lockout (UVLO)

This circuit insures that V_{CC} is adequate to make the UC3842 fully operational before enabling the output stage. Figure 5a shows that the UVLO turn-on and turn-off thresholds are fixed internally at 16V and 10V respectively. The 6V hysteresis prevents V_{CC} oscillations during power sequencing. Figure 5b shows supply current requirements. Start-up current is less than 1mA for efficient bootstrapping from the rectified input of an off-line converter, as illustrated by Figure 6. During normal circuit operation, V_{CC} is developed from auxiliary winding W_{AUX} with D_1 and C_{IN}. At start-up, however, C_{IN} must be charged to 16V through R_{IN}. With a start-up current of 1mA, R_{IN} can be as large as 100kΩ and still charge C_{IN} when V_{AC} = 90V RMS (low line). Power dissipation in R_{IN} would then be less than 350mW even under high line (V_{AC} = 130V RMS) conditions.

During UVLO, the UC3842 output driver is biased to a high impedance state. However, leakage currents (up to 10μA), if not shunted to ground, could pull high the gate of a POWERMOS. A 100kΩ shunt, as showing in Figure 6, will hold the gate voltage below 1V.

Fig. 5 (a) - Under-voltage lockout and (b) supply current requirements.

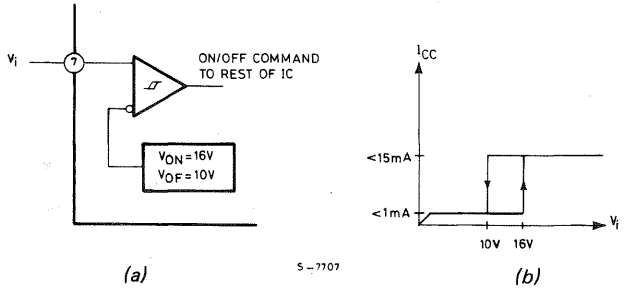
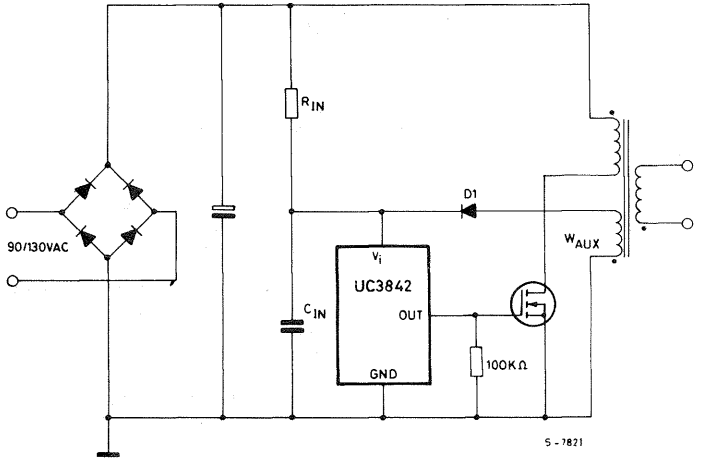


Fig. 6 - Providing power to the UC3842



Oscillator

The UC3842 oscillator is programmed as shown in Figure 7a. Oscillator timing capacitor C_T is charged from V_{REF} (5V) through R_T, and discharged by an internal current source. Charge and discharge times are given by:

$$t_c \approx 0.55\, R_T\, C_T$$

$$t_d \approx R_T\, C_T\, \ell n \left(\frac{0.0063\, R_T - 2.7}{0.0063\, R_T - 4.0} \right)$$

frequency, then, is: $f = \dfrac{1}{t_c + t_d}$

For $R_T > 5k\Omega$, t_d is small compared to t_c, and:

$$f \approx \frac{1}{0.55\, R_T\, C_T} \approx \frac{1.8}{R_T\, C_T}$$

During the discharge time, the internal clock signal blanks the output to the low state. Therefore, t_d limits maximum duty cycle (D_{MAX}) to:

$$D_{MAX} = \frac{t_c}{t_c + t_d} = 1 - \frac{t_d}{\tau}$$

where: $\tau = 1/f$ = switching period.

The timing capacitor discharge current is not tightly controlled, so t_d may vary somewhat over temperature and from unit to unit. Therefore, when very precise duty cycle limiting is required, the circuit of Figure 7b is recommended.

One or more UC3842 oscillators can be synchronized to an external clock as shown in Figure 8. Noise immunity is enhanced if the free-running oscillator frequency ($f = 1/(t_c + t_d)$) is programmed to be ~ 20% less than the clock frequency.

Fig. 7 (a) - Oscillator timing connections and (b) circuit for limiting duty cycle.

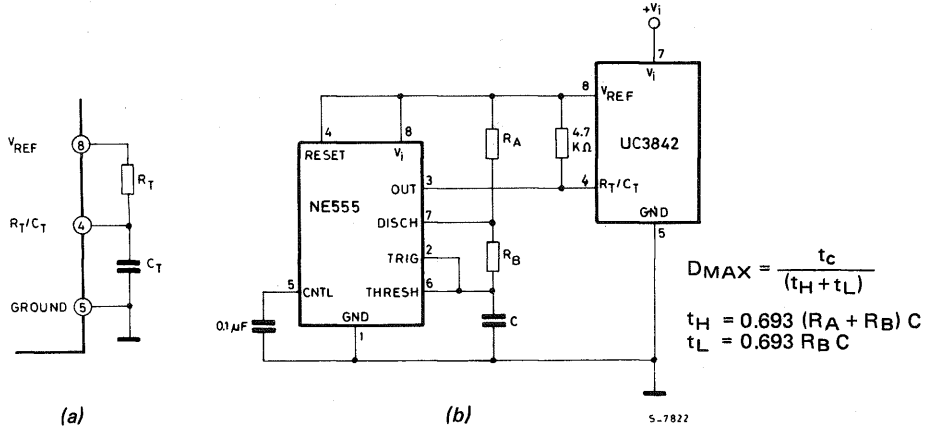
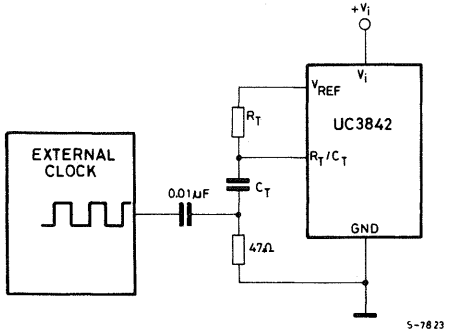


Fig. 8 - Synchronization to an external clock



Error Amplifier

The error amplifier (E/A) configuration is shown in Figure 9. The non-inverting input is not brought out to a pin, but is internally biased to 2.5V ± 2%. The E/A output is available at pin 1 for external compensation, allowing the user to control the converter's closed-loop frequency response.

Figure 10a shows an E/A compensation circuit suitable for stabilizing any current-mode controlled topology except for flyback and boost converters operating with continuous inductor current. The feedback components add a pole to the loop transfer function at $f_p = 1/2\pi\, R_f\, C_f$. R_f and C_f are chosen so that this pole cancels the zero of the output filter capacitor ESR in the power circuit. R_i and R_f fix the low-frequency gain. They are chosen to provide as much gain as possible while still allowing the pole formed by the output filter capacitor and load to roll off the loop gain to

unity (0dB) at f ≈ $f_{switching}/4$. This technique insures converter stability while providing good dynamic response.

Continuous-inductor-current boost and flyback converters each have a right-half-plane zero in their transfer function. An additional compensation pole is needed to roll off loop gain at a frequency less than that of the RHP zero. R_p and C_p in the circuit of Figure 10b provide this pole.

The E/A output will source 0.5mA and sink 2mA. A lower limit for R_f is given by:

$$R_{f(MIN)} \approx \frac{V_{E/A\ OUT(MAX)} - 2.5V}{0.5mA} = \frac{6V - 2.5V}{0.5mA} = 7k\Omega$$

E/A input bias current (2μA max) flows through R_i, resulting in a DC error in output voltage (V_O) given by:

$$\Delta V_{O(MAX)} = (2\mu A)\ R_i$$

It is therefore desirable to keep the value of R_i as low as possible.

Figure 11 shows the open-loop frequency response of the UC3842 E/A. The gain represent an upper limit on the gain of the compensated E/A. Phase lag increases rapidly as frequency exceeds 1MHz due to second-order poles at ~ 10MHz and above.

Fig. 9 - UC3842 error amplifier

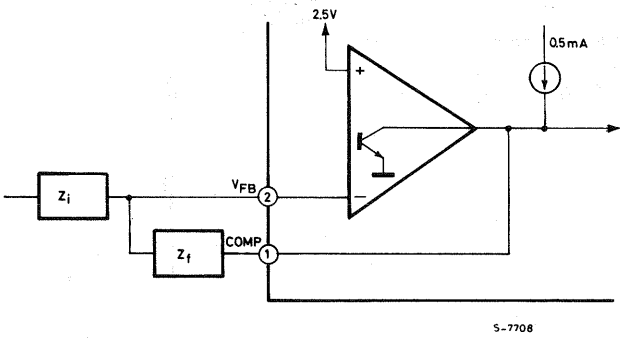
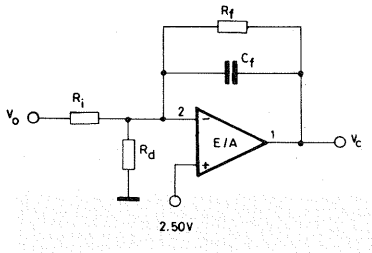
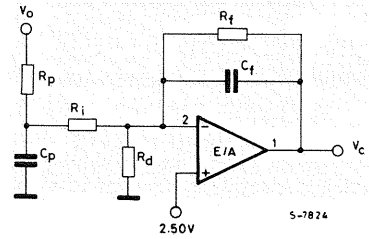


Fig. 10 - (a) Error amplifier compensation addition pole and (b) needed for continuous inductor-current boost ad flyback.

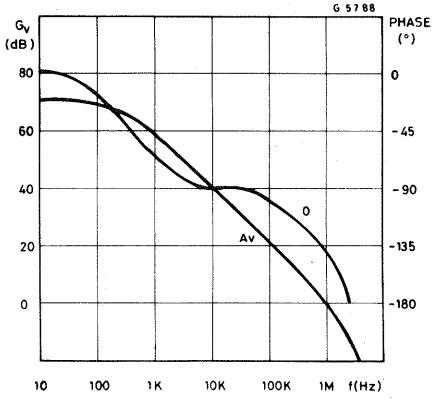


(a)



(b)

Fig. 11 - Error amplifier open-loop frequency response



Current Sensing and Limiting

The UC3842 current sense input is configured as shown in Figure 12. Current-to-voltage conversion is done externally with ground-referenced resistor R_S. Under normal operation the peak voltage across R_S is controlled by the E/A according to

the following relation:

$$V_{R_S(pk)} = \frac{V_C - 1.4V}{3}$$

where: V_C = control voltage = E/A output voltage.

R_S can be connected to the power circuit directly or through a current transformer, as Figure 13 illustrates. While a direct connection is simpler, a transformer can reduce power dissipation in R_S, reduce errors caused by the base current, and provide level shifting to eliminate the restraint of ground-referenced sensing. The relation between V_C and peak current in the power stage is given by:

$$i_{(pk)} = N\left(\frac{V_{R_S(pk)}}{R_S}\right) = \frac{N}{3R_S}\left(V_C - 1.4V\right)$$

where: N = current sense transformer turns ratio.
= 1 when transformer not used.

For purposes of small-signal analysis, the control-to-sensed-current gain is:

$$\frac{i_{(pk)}}{V_C} = \frac{N}{3R_S}$$

When sensing current in series with the power transistor, as shown in Figure 13, current waveform will often have a large spike at its leading edge. This is due to rectifier recovery and/or inter-winding capacitance in the power transformer. If unattenuated, this transient can prematurely terminate the output pulse. As shown, a simple RC filter is usually adequate to suppress this spike. The RC time constant should be approximately equal to the current spike duration (usually a few hundred nanoseconds).

The inverting input to the UC3842 current-sense comparator is internally clamped to 1V (Figure 12). Current limiting occurs if the voltage at pin 3 reaches this threshold value, i.e. the current limit is defined by:

$$i_{MAX} = \frac{N \cdot 1V}{R_S}$$

Fig. 12 - Current sensing

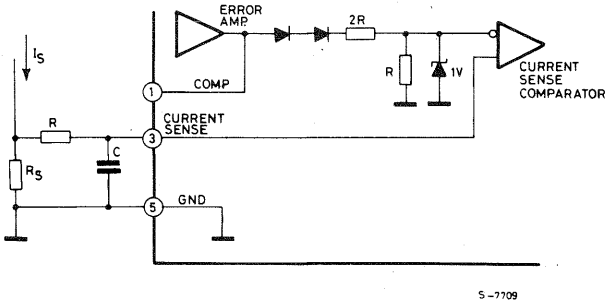
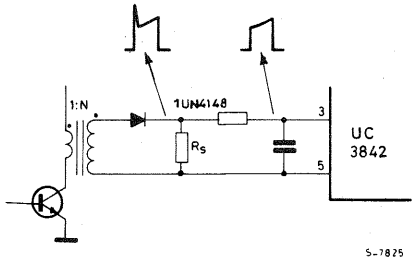


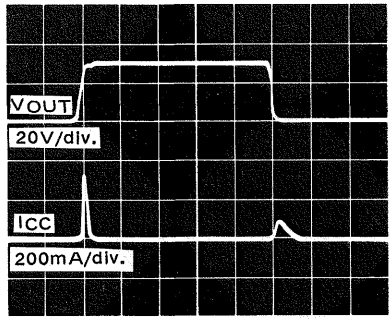
Fig. 13 - Transformer-coupled current sensing



Totem-Pole Output

The UC3842 has a single totem-pole output. The output transistors can be operated to ± 1A peak current and ± 200mA average current. The peak current is self-limiting, so no series current-limiting resistor is needed when driving a power MOS gate. Cross-conduction between the output transistors is minimal, as Figure 14 shows. The average added power due to cross-conduction with V_i = 30V is only 80mW at 200kHz.

Fig. 14 - Output cross-conduction



Figures 15-17 show suggested circuits for driving POWERMOS and bipolar transistors with the UC3842 output. The simple curcuit of Figure 15 can be used when the control IC is not electrically isolated from the power MOS. Series resistor R_1 provides damping for a parasitic tank circuit formed by the power MOS input capacitance and any series wiring inductance. Resistor R_2 shunts output leakage currents (10μA maximum) to ground when the under-voltage lockout is active. Figure 16 shows an isolated power MOS drive circuit which is appropriate when the drive signal must be level-shifted or transmitted across an isolation boundary. Bipolar transistors can be driven effectively with the circuit of Figure 17. Resistors R_1 and R_2 fix the on-state base current. Capacitor C_1 provides a negative base current pulse to remove stored charge at turn-off.

Fig. 15 – Direct POWERMOS drive

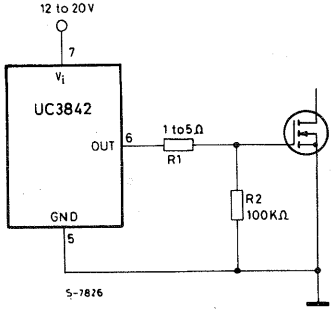


Fig. 16 – Isolated POWERMOS drive

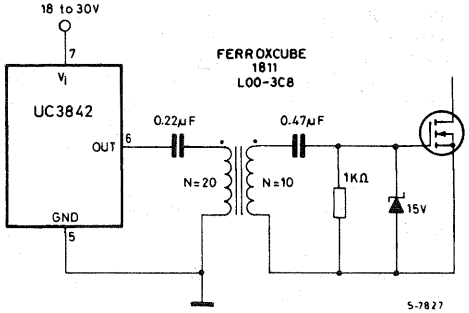
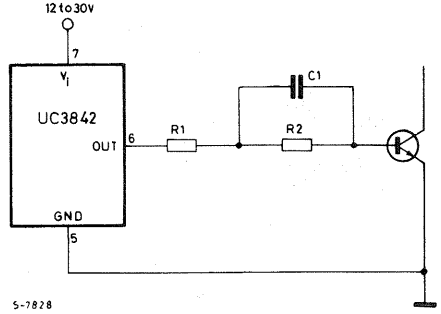


Fig. 17 – Bipolar drive with negative turn-off bias



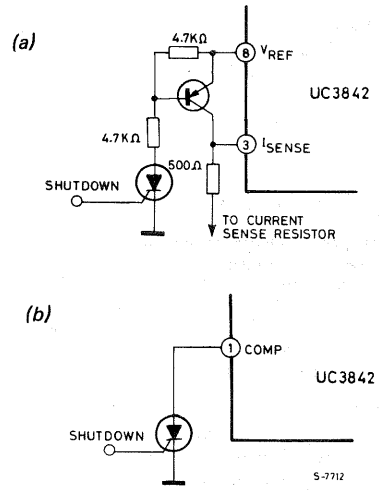
PWM Latch

This flip-flop, shown in Figure 4, ensures that only a single pulse appears at the UC3842 output in any one oscillator period. Excessive power transistor dissipation and potential saturation of magnetic elements are thereby averted.

Shutdown Techniques

Shutdown of the UC3842 can be accomplished by two methods; either raise pin 3 above 1V or pull pin 1 below 1V. Either method causes the output of the PWM comparator to be high (refer to block diagram, Figure 4). The PWM latch is reset dominant so that the output will remain low until the first clock pulse following removal of the shutdown signal at pin 1 or pin 3. As shown in Figure 18, an externally latched shutdown can be accomplished by adding an SCR which will be reset by cycling V_{CC} below the lower under-voltage lockout threshold (10V). At this point all internal bias is removed, allowing the SCR to reset.

Fig. 18 – Shutdown achieved by
a) Pulling pin 3 high
b) Pulling pin 1 Low



AVOIDING COMMON PITFALLS

Current-mode controlled converters can exhibit performance peculiarities under certain operating conditions. This section explains these situations and how to correct them when using the UC3842.

Slope Compensation Prevents Instabilities

It is well documented that current-mode controlled converters can exhibit subharmonic oscillations

when operated at duty cycles greater than 50% .

Fortunately, a simple technique (usually requiring only a single resistor to implement) exists which corrects this problem and at the same time improves converter performance in other respects. This "slope compensation" technique is described in detail in Reference 6. It should be noted that "duty cycle" here refers to output pulse width divided by oscillator period, even in push-pull designs where the transformer period is twice that of the oscillator. Therefore, push-pull circuits will almost always require slope compensation to prevent subharmonic oscillation.

Figure 19 illustrates the slope compensation technique. In Figure 19a the uncompensated control voltage and current sense waveforms are shown as a reference. Current is often sensed in series with the switching transistor for buck-derived topologies. In this case, the current sense signal does not track the decaying inductor current when the transistor is off, so dashed lines indicate this inductor current. The negative inductor current slope is fixed by the values of output voltage (V_O) and inductance (L):

$$\frac{di_L}{dt} = \frac{V_L}{L} = \frac{-V_F - V_O}{L} = \frac{-(V_F + V_O)}{L}$$

where: V_F = forward voltage drop across the freewheeling diode. The actual slope (m_2) of the dashed lines in Figure 19a is given by:

$$m_2 = \frac{R_S}{N} \cdot \frac{di_L}{dt} = \frac{-R_S (V_F + V_O)}{NL}$$

where: R_S and N are defined as the "Current Sensing" section of this paper.

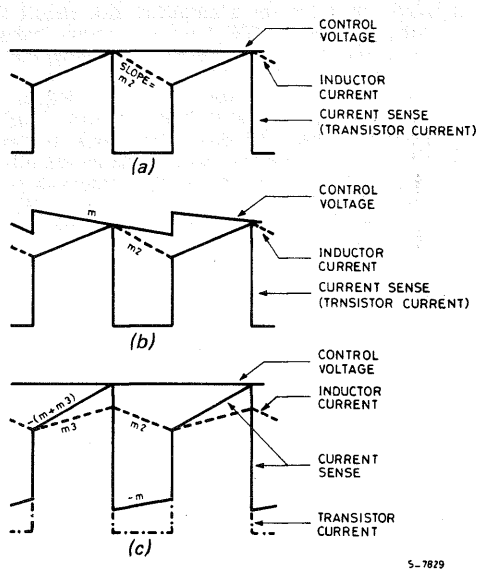
In Figure 19b, a sawtooth voltage with slope m has been added to the control signal. The sawtooth is synchronized with the PWM clock, and practice is most easily derived from the control chip oscillator as shown in Figure 20a. The sawtooth slope in Figure 19b is $m = m_2/2$ This particular slope value is significant in that it yields "perfect" current-mode control; i.e. with $m_2/2$ the average inductor current follows the control signal so that, in the small-signal analysis, the inductor acts as a controlled current source. All current-mode controlled converters having continuous inductor current therefore benefit from this amount of slope compensation, whether or not they operate above 50% duty.

More slope is needed to prevent subharmonic oscillations at high duty cycles. With slope $m = m_2$, such oscillations will not occur if the error amplifier gain ($A_{V(E/A)}$) at half the switching frequency ($f_s/2$) is kept below a threshold value (Reference 6):

$$A_{V(E/A)} \Big|_{\substack{m = m_2 \\ f = f_s/2}} < \frac{\pi^2 C_O}{4\tau}$$

where: C_O = sum of filter and load capacitance
$\tau = 1/f_s$

Fig. 19 - Slope compensation waveforms:
a) No Comp.
b) Comp. added to control voltage
c) Comp. added to current sense



Slope compensation can also improve the noise immunity of a current-mode controlled supply. When the inductor ripple current is small compared to the average current (as in Figure 19a), a small amount of noise on the current sense or control signals can cause a large pulse-width jitter. The magnitude of this jitter varies inversely with the difference in slope of the two signals. By adding slope as in Figure 19b, the jitter is reduced. In noisy environments it is sometimes necessary to add slope $m > m_2$ in order to correct this problem. However, as m increases beyond $m = m_2/2$, the circuit becomes less perfectly current controlled. A complex trade-off is then required; for very noisy circuits the optimum amount of slope compensation is best found empirically.

Once the required slope is determined, the value of R_{SLOPE} in Figure 20a can be calculated:

$$3\,m = \frac{\Delta V_{RAMP}}{\Delta t_{RAMP}} \cdot A_{V(E/A)} = \frac{0.7V}{\tau/2}\left(\frac{R_{SLOPE}}{Z_F|f_s}\right) = \frac{1.4}{\tau}\left(\frac{R_{SLOPE}}{Z_F|f_s}\right)$$

$$R_{SLOPE} = \frac{3m\tau}{1.4}(Z_F|f_s) = 2.1 \cdot m \cdot \tau \cdot Z_F|f_s$$

where: $Z_F|f_s$ is the E/A feedback impedance at the switching frequency.

For $m = m_L$: $\Delta\tau_{RAMP}$

$$R_{SLOPE} = 1.7\tau\left(\frac{R_S (V_F + V_O)}{NL}\right) Z_F|f_s$$

Note that in order for the error amplifier to accurately replicate the ramp, Z_F must be constant over the frequency range f_s to at least $3f_s$.

In order to eliminate this last constraint, an alternative method of slope compensation is shown in Figures 19c and 20b. Here the artificial slope is added to the current sense waveform rather than subtracted from the control signal. The magnitude of the added slope still relates to the downslope of inductor current as described above. The requirement for R_{SLOPE} is now:

$$m = \frac{\Delta V_{RAMP}}{\Delta t_{RAMP}}\left(\frac{R_f}{R_f + R_{SLOPE}}\right) = \frac{0.7}{\tau/2}\left(\frac{R_f}{R_f + R_{SLOPE}}\right)$$

$$R_{SLOPE} = \frac{1.4\,R_f}{m\tau} - R_f = R_f\left(\frac{1.4}{m\tau} - 1\right)$$

For $m = m_2$:

$$R_{SLOPE} = R_f\left(\frac{1.4NL}{R_S\,(V_F + V_O)\,\tau} - 1\right)$$

R_{SLOPE} loads the UC3842 R_T/C_T terminal so as to cause a decrease in oscillator frequency. If $R_{SLOPE} >> R_T$ then the frequency can be corrected by decreasing R_T slightly. However, with $R_{SLOPE} \lesssim 5R_T$ the linearity of the ramp degrades noticeably, causing over-compensation of the supply at low duty cycles. This can be avoided by driving R_{SLOPE} with an emitter-follower as shown in Figure 21.

Fig. 20 - Slope compensation added (a) to control signal or (b) to current sense waveform

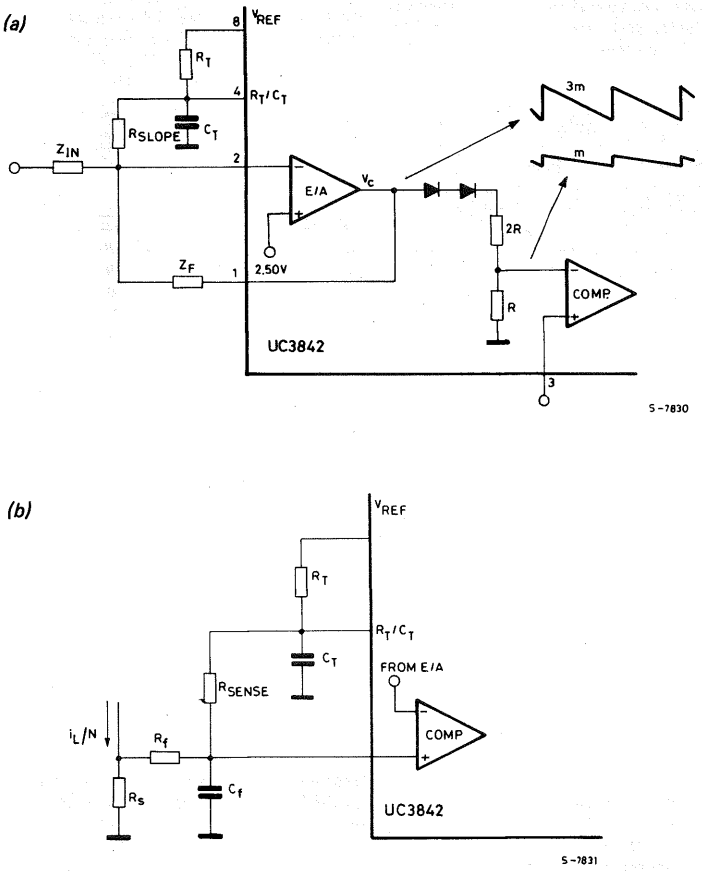
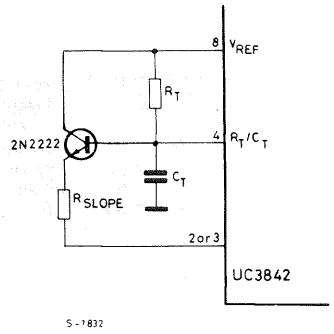


Fig. 21 - Emitter-follower minimizes load at RT/CT terminal.



Noise

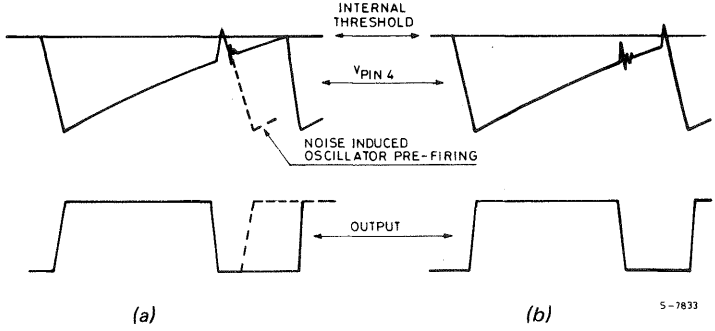
As mentioned earlier, noise on the current sense or control signals can cause significant pulse-width jitter, particularly with continuous-inductor-current designs. While slope compensation helps alleviate this problem, a better solution is to minimize the amount of noise. In general, noise immunity improves as impedance decrease at critical points in a circuit.

One such point for a switching supply is the ground line. Small wiring inductances between various ground points on a PC board can support common-mode noise with sufficient amplitude to interfere with correct operation of the modulating IC. A copper ground plane and separate return lines for high-current paths greatly reduce common-mode noise. Note that the UC3842 has a single ground pin. High sink currents in the output therefore cannot be returned separately.

Ceramic bypass capacitors (0.1μF) from V_i and V_{REF} to ground will provide low-impedance paths for high frequency transients at those points. The input to the error amplifier, however, is a high-impedance point which cannot be bypassed without affecting the dynamic response of the power supply. Therefore, care should be taken to lay out the board in such a way that the feedback path is far removed from noise generating components such as the power transistor(s).

Figure 22a illustrates another common noise-induced problem. When the power transistor turns off, a noise spike is coupled to the oscillator R_T/C_T terminal. At high duty cycles the voltage at R_T/C_T is approaching its threshold level (~2.7V, established by the internal oscillator circuit) when this spike occurs. A spike of sufficient amplitude will prematurely trip the oscillator as shown by the dashed lines. In order to minimize the noise spike, choose C_T as large as possible, remembering that deadtime increases with C_T. It is recommended that C_T never be less than ~1000pF. Often the noise which causes this problem is caused by the output (pin 6) being pulled below ground at turn-off by external parasitics. This is particularly true when driving POWERMOS. A diode clamp from ground to pin 6 will prevent such output noise from feeding to the oscillator. If these measures fail to correct the problem, the oscillator frequency can always be stabilized with an external clock. Using the circuit of Figure 8 results in an R_T/C_T waveform like that of Figure 22b. Here the oscillator is much more immune to noise because the ramp voltage never closely approaches the internal threshold.

Fig. 22 - a) Noise on pin 4 can cause oscillator to pre-trigger
b) With external sync. noise does not approach threshold level

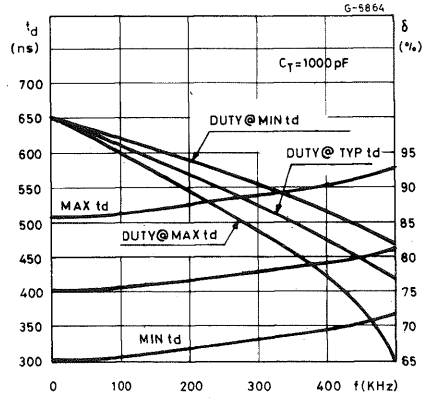


Maximum Operating Frequency

Since output deadtime varies directly with C_T, the restraint on minimum C_T (1000pF) mentioned above results in a minimum deadtime capability for the UC3842. This minimum deadtime varies with R_T and therefore with frequency, as shown in Figure 23. Above 100kHz, the deadtime significantly reduces the maximum duty cycle obtainable at the UC3842 output (also show in Figure 23). Circuits not requiring large duty cycles, such as the forward converter and flyback topologies, could operate as high as 500kHz. Operation at higher frequencies is not recommended because the deadtime become less predictable.

The speed of the UC3842 current sense section poses an additional constraint on maximum operating frequency. A maximum current sense delay of 400ns represents 10% of the switching period at 250kHz and 20% at 500kHz. Magnetic components must not saturate as the current continues to rise during this delay period, and power semiconductors must be chosen to handle the resulting peak currents. In short, above ~250kHz, may of the advantages of higher-frequency operation are lost.

Fig. 23 - Deadtime and maximum obtainable duty-cycle vs. frequency with minimum recommended CT.



CIRCUIT EXAMPLES

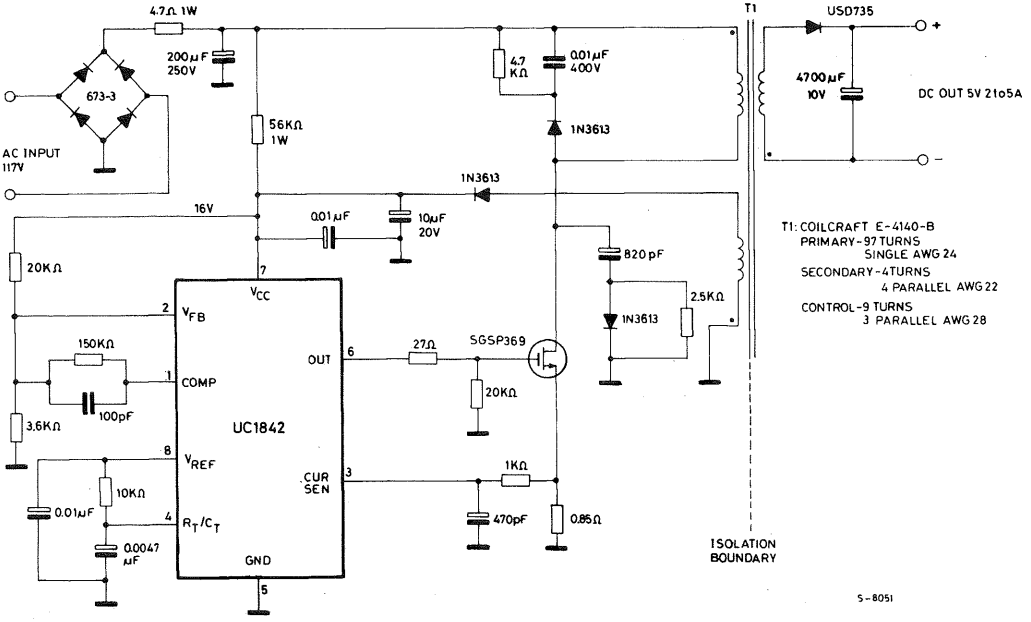
1. Off-Line Flyback

Figure 24 shows a 25W multiple-output off-line flyback regulator controlled with the UC3842. This regulator is low in cost because it uses only two magnetic elements, a primary-side voltage sensing technique, and an inexpensive control circuit. Specifications are listed below.

SPECIFICATIONS:

Input Voltage	95 VAC to 130 VAC (50Hz/60Hz)
Output Voltage:	A. +5V, 5%: 1A to 4A load Ripple voltage: 50mV P-P Max.
	B. +12V, 3% : 0.1A to 0.3A load Ripple voltage: 100mV P-P Max
	C. -12V, 3% 0.1A to 0.3A load Ripple voltage: 100mV P-P Max
Line Isolation:	3750V
Switching Frequency:	40kHz
Efficiency @ full load:	70%

Fig. 24 - 25W off-line flyback regulator



A NEW INTEGRATED CIRCUIT FOR CURRENT-MODE CONTROL

Reprinted from the Proceedings of Powercon10
March 22-24, 1983 • San Diego, California

The inherent advantages of current-mode control over conventional PWM approaches to switching power converters read like a wish list from a frustrated power supply design engineer. Features such as automatic feed forward, automatic symmetry correction, inherent current limiting, simple loop compensation, enhanced load response, and the capability for parallel operation all are characteristics of current-mode conversion. This paper introduces the first control integrated circuit specifically designed for this tipology, defines its operation and describes practical examples illustrating its use and benefits.

INTRODUCTION

Over the past several years an increased interest in current-mode control of switching inverters has surfaced in the literature. Originally inverted in the late 1960s, this scheme was not publicly reported until 1977 (1) and has seen rapid development by many authors to date (2-6). In short, current-mode control uses an inner or secondary loop to directly control peak inductor current with the error signal rather than controlling duty ratio of the pulse width modulator as in conventional converters. Practically, this means that instead of comparing the error voltage to a voltage ramp, it is compared to an analogue of the inductor current forcing the peak current to follow the error voltage.

Fig. 1 - A fixed frequency current-mode controlled regulator.

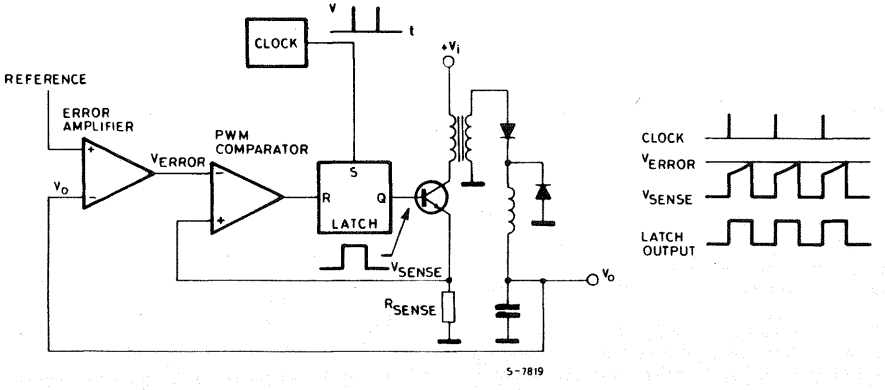
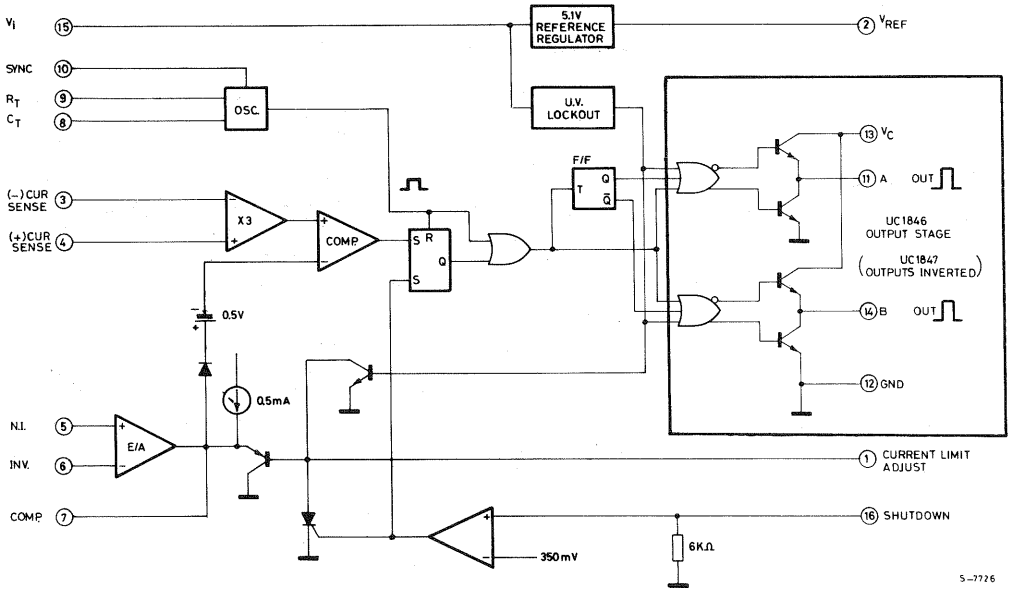


Figure 1 illustrates a simplified block diagram of a fixed frequency buck regulator employing current-mode control. As shown, the error signal, V_o, is controlling peak switch current which, to a good approximation, is proportional to average inductor current. Since the average inductor current can change only if the error signal changes, the inductor may be replaced by a current source, and the order of the system reduced by one. This results in a number of performance advantages including improved transient response, a simpler, more easily designed control loop, and line regulation comparable to conventional feed-forward schemes. Peak current sensing will automatically provide flux balancing thereby eliminating the need for complex balance schemes in push-pull systems. Additionally, by simply limiting the peak swing of the error voltage V_o, instantaneous peak current limiting is accomplished. Lastly, by feeding identical power stages with a common error signal, outputs may be paralleled while maintaining equal current sharing.

Although the advantages of current-mode control are abundant, wide acceptance of this technique has been hampered by a lack of suitable integrated circuits to perform the associated control functions. This paper introduces a new integrated circuit designed specifically for control of current-mode converters. Circuit function and features are described in detail, and a comparative design example is used to illustrate the numerous advantages of this approach.

Fig. 2 - UC1846 Block Diagram.



UC1846 CHIP ARCHITECTURE

In addition to all the functions required of conventional PWM controllers, a current-mode controller must be able to sense switch or inductor current and compare it on a pulse-by-pulse basic with the output of the error amplifier. As may be seen in the block diagram of Figure 2, this is accomplished in the UC1846 by using a differential current sense amplifier with a fixed gain of 3. The amplifier allows sensing of low level voltages while maintaining high noise immunity. A list of other features, while not unique to current-mode conversions, demonstrates the advanced, state-of-the-art architecture of the UC1846:

- A ± 1%, 5.1V trimmed bandgap reference used both as an external voltage reference and internal regulated power source to drive low level circuitry.
- A fixed frequency sawtooth oscillator with variable deadtime control and external synchronization capability. Circuitry features an all NPN design capable of producing low distortion waveforms well in excess of 1MHz.
- An error amplifier with common mode range from ground to V_{cc}-2V.

- Current limiting through clamping of the error signal at a user-programmed level.
- A shutdown function with built in 350mV threshold. May be used in either a latching, or non-latching mode. Also capable of initiating a "hiccup" mode of operation.
- Under-voltage lockout with hysteresis to guarantee outputs will stay "off" until reference is in regulation.
- Double pulse suppression logic to eliminate the possibility of consecutively pulsing either output.
- Totem pole output stages capable of sinking or sourcing 100mA continuous. 400mA peak currents.

These various features, along with their interrelationships and applications to switched-mode regulators, will be further discussed in the following sections.

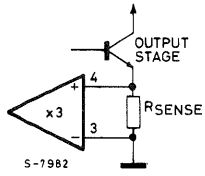
UC1846 FUNCTIONAL DESCRIPTION

Current Sense Amplifier

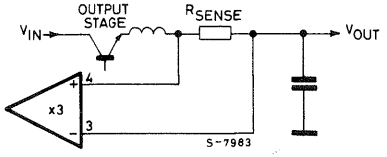
The current sense amplifier may be used in a variety of ways to sense peak switch current for comparison with an error voltage. Referring to Figure 2, maximum swing on the inverting input of the PWM comparator is limited to approximately 3.5V by the internal regulated supply. Accordingly, for a fixed gain of 3, maximum differential voltages must be kept below 1.2V at the current sense inputs. Figure 3 depicts several methods of configuring sense schemes. Direct resistive sensing is simplest, however, a lower peak voltage may be required to minimize power loss in the sense resistor. Transformer coupling can provide isolation and increase efficiency at the cost of added complexity. Regardless of scheme, the largest sense voltage consistent with low power losses should be chosen for noise immunity. Tipically, this will range from several hundred millivolts in some resistive sense circuits to the maximum of 1.2V in transformer coupled circuits.

In addition, caution should be exercised when using a configuration that senses switch current (Figure 3A) instead of inductor current (Figure 3B). As the switch is turned on, a large instantaneous current spike can be generated in the sense resistor as the collector capacitance of the switch is discharged. This spike will often be of sufficient magnitude and duration to trip the current sense latch and result in erratic operation of the PWM circuit, particularly at lower duty cycles. A small RC filter (Figure 4) in series with the input is generally all that is required to reduce the spike to an acceptable level.

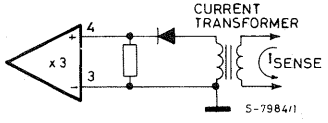
Fig. 3 - Various current sense schemes.



A) Resistive sensing with ground reference.

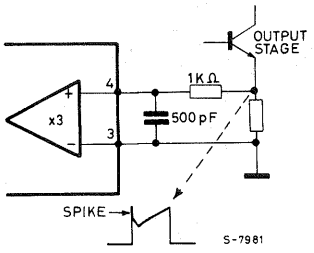


B) Resistive sensing above ground.



C) Isolated current sensing.

Fig. 4 - RC filter for reducing switch transients.



Oscillator

Although many data sheets tout 300 to 500KHz operation, virtually all PWM control chips suffer from both poor temperature characteristics and waveforms distortions all these frequencies. Practical usage is generally limited to the 100 to 200KHz range. This is a direct consequence of having slow (f_t = 2MHz) PNP transistors in the oscillator signal path. By implementing the oscillator using all NPN transistors, the UC1846 achieves excellent temperature stability and waveform clarity at frequencies in excess of 1MHz.

Referring to Figure 5, an external resistor R_T is used to generate a constant current into a capacitor C_T to produce a linear sawtooth waveform. Oscillator frequency may be approximated by selecting R_T and C_T such that

$$f_{OSC} = \frac{2.2}{R_T C_T} \qquad (1)$$

Where R_T can range from 1KΩ to 500KΩ and C_T is above 100pF. For quick reference a plot of frequency versus R_T and C_T is given in Figure 6.

Fig. 5 – Oscillator circuit

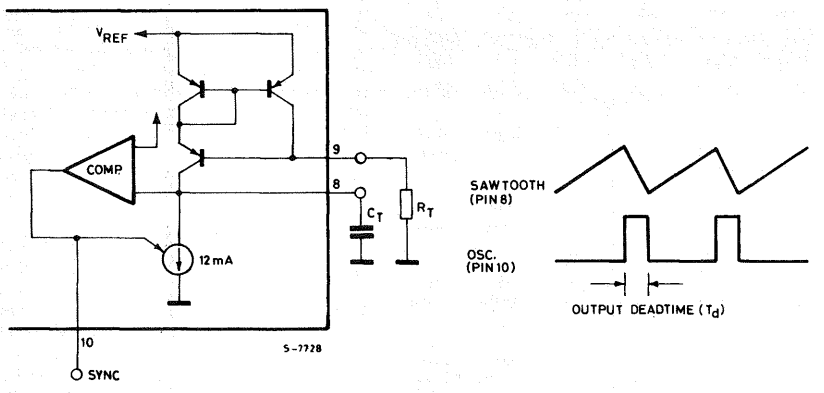


Fig. 6 – Oscillator frequency as a function of RT and CT.

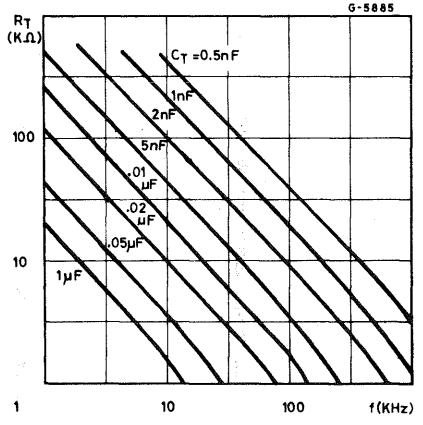


Fig. 7 – Output deadtime as a function of timing capacitor CT

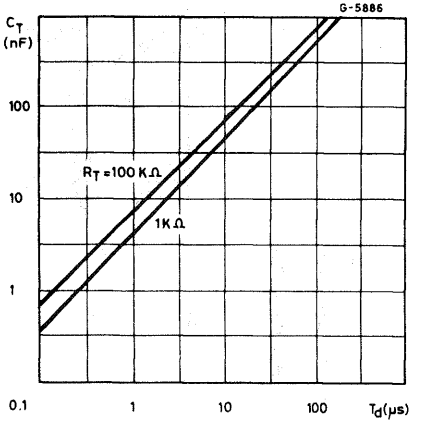
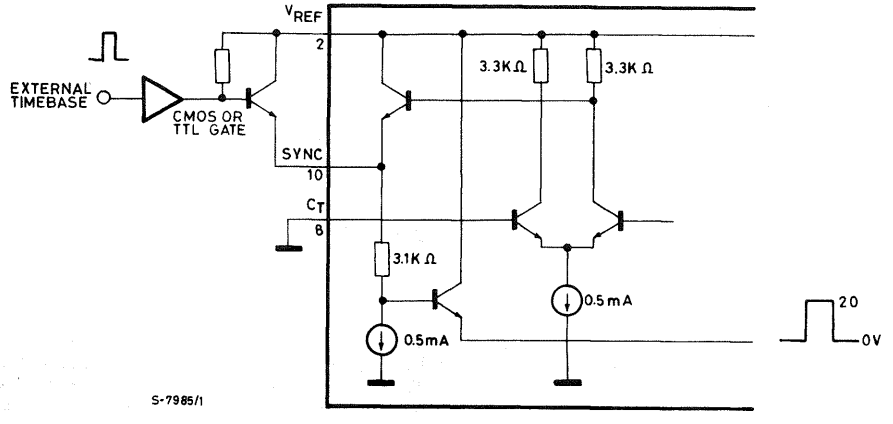


Fig. 8 – Synchronizing the 1846 to an external time base.



Again referring to Figure 5, the oscillator generates an internal clock pulse used, among other things, to blank both outputs and prevent simultaneous cross conduction during switching transitions. This output "deadtime" is controlled by the oscillator fall time. Fall time, in turn, is controlled by C_T according to the formula:

$$\tau d = 145\ C_T \left[\frac{12}{12 - 3.6/R_T\,(k\Omega)} \right] \qquad (2)$$

For large values of R_T

$$\tau d = 145\ C_T \qquad (3)$$

A plot of output deadtime versus C_T for two values of R_T is given in Figure 7.

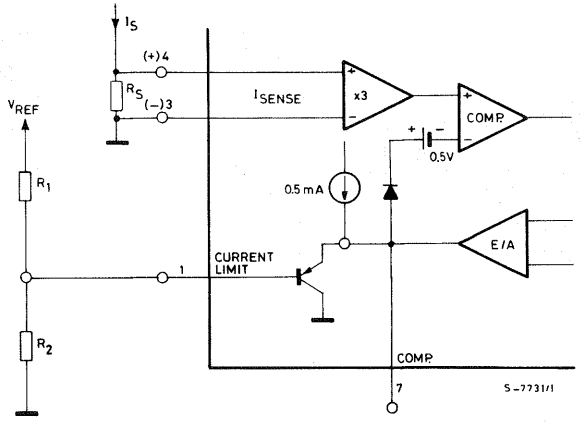
Although timing capacitors as small as 100pF can be used successfully in low noise environments, it is generally recommended that C_T be kept above 1000pF to minimize noise effects on the oscillator frequency.

Synchronization of one or more devices to either an external time base or another UC1846 is accomplished via the bi-directional SYNC pin. To synchronize devices, first, C_T must be grounded to disable the internal oscillator on all slaved devices. Second, an external synchronization pulse must be applied to the SYNC terminal. This pulse can come directly from the SYNC terminal of a master UC1846 or, alternatively, from an external time base as shown in Figure 8.

Current Limit

One of the most attractive features of a current-mode converter is its ability to limit peak switch currents on a pulse-by-pulse basis by simply limiting the error voltage to a maximum value. Referring to Figure 9, peak current limiting in the UC1846 is accomplished using a divider network, R_1 and R_2, to set a pre-determined voltage at pin 1.

Fig. 9 - Peak current limit set up.



This voltage, in conjuction with Q_1, acts to clamp the output of the error amplifier at a maximum value. Since the base emitter drop of Q_1, and the forward drop of diode D_1 very nearly cancel, the negative input of the comparator will be clamped at the value $V_{PIN\ 1}$ -0.5V. Following this through to the input of the current sense amplifier yields.

$$V_{CS} = \frac{V_{PIN\ 1} - 0.5}{3} \qquad (4)$$

Where V_{CS} is the differential input voltage of the current sense amplifier. Using this relationship, a value for maximum switch current in terms of external programming resistors can be derived, resulting in:

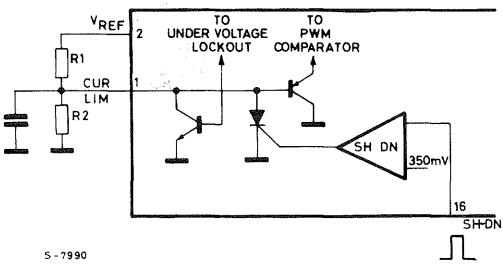
$$I_{CL} = \frac{\dfrac{R_2\ V_{REF}}{R_1 + R_2} - 0.5}{3R_S} \qquad (5)$$

While still on the subject of resistor selection, it should be pointed out that R_1 also supplies holding current for the shutdown circuit, and therefore should be selected prior to selecting R_2 as outlined in the next section.

One last word on the current limit circuit. As may be seen from equation 5, any signal less than 0.5V at the current limit input will guarantee both outputs to be off, making pin 1 a convenient point for both shutting down and slow starting the PWM

circuit. For example, both the under-voltage lockout and shutdown functions are connected internally to this point. If a capacitor is used to hold pin 1 low (Figure 10) then as the input voltage increases above the under-voltage lockout level, the capacitor will charge and gradually increase the PWM duty cycle to its operating point. In a similar manner if the shutdown amplifier is pulsed, the shutdown SCR will be fired and the capacitor discharged, guaranteeing a shutdown and soft restart cycle independent of input pulse width.

Fig. 10 - Using under-voltage lockout and shutdown to initiate a slow start.



Shutdown

The shutdown circuit, shown in Figure 11, was designed to provide a fast acting general purpose shutdown port for use in implementing both protection circuitry and remote shutdown functions. The circuit may be divided into an input section consisting of a comparator with a 350mV temperature compensated offset, and an output section consisting of a three transistor latch. Shutdown is accomplished by applying a signal greater than 350mV to pin 16, causing the output latch to fire, and setting the PWM latch to provide an immediate signal to the outputs. At this point, several things can happen. Q_1 requires a minimum holding current, I_H, of approximately 1.5mA to remain in the latched state. Therefore, if R_1 is chosen greater than 5kΩ, Q_1 will discharge any capacitance, C_S, on pin 1 to ground and commutate the output latch, allowing C_S to recharge. If R_1 is chosen less than 2.5kΩ. Q_1 will discharge C_S and remain in the latched state until power is externally cycled off. In either case, C_S is required only if a soft-start or soft-restart function is desired.

For example, the shutdown circuit of Figure 12, operating in a nonlatched mode, will protect the supply from overcurrent fault conditions. Many times, if the output of a supply is shorted, circulating currents in the output inductor will build to dangerous levels. Pulse-by-pulse current limiting with its inherent time delay, will in general not be able to limit these currents to acceptable levels. Figure 12 details a circuit which will provide shutdown and soft-restart if the overcurrent threshold set by R_3 and R_4 is exceeded. This level should be greater than the peak current limit value determined by R_1 and R_2 (see equation 5). Sometimes called a "hiccup mode", this overcurrent function will limit both power and peak current in the output stages until the fault is removed.

Fig. 11 - Shutdown circuitry.

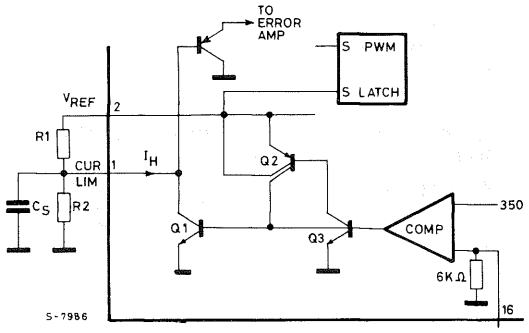
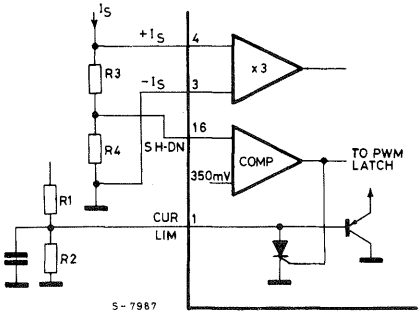


Fig. 12 - Over current sensing with the shutdown circuit produces a shutdown - soft restart cycle to protect output drivers.



NOISE IMMUNITY

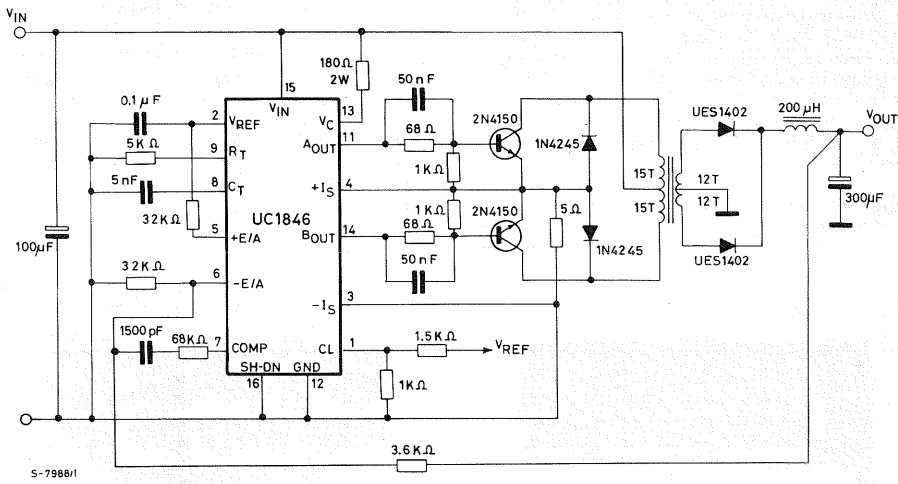
As in all PWM circuits, some simple precautions should be observed to prevent switching noise from prematurely triggering the oscillator as it approaches its upper threshold. This is most evident when large capacitive loads — such as the gate of POWER MOS — are directly driven from outputs A and B. As the duty cycle approaches 100%, the current spike associated with this output capacitance can cause the oscillator to prematurely trigger with a resulting shift upward in frequency. By separating high current ground paths from low level analog grounds, using C_T values greater than 1000pF grounded directly to pin 12, and decoupling both V_i and V_{REF} with good quality bypass capacitors, noise problems can be avoided.

COMPARATIVE DESIGN EXAMPLE

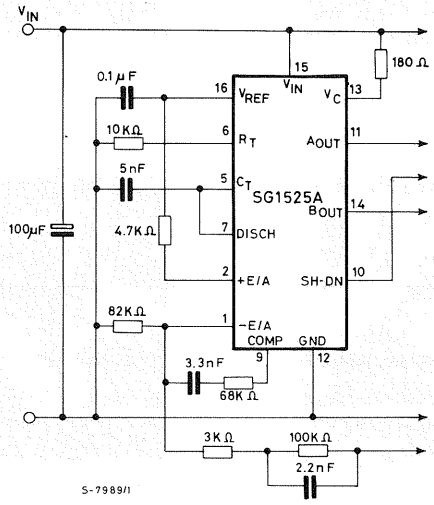
To more vividly illustrate the advantages of current-mode control, a relatively simple push-pull forward converter was designed using two interchangeable control sections, as shown in Figure 13. The control modules consist of (a) a UC1846 current-mode controller with associated circuitry, and (b) a conventional SG1525A PWM controller with its support circuitry. Loop compensation of the SG1525A was implemented by placing a zero in the feedback loop to cancel one of the poles in the output stage, resulting in a unity gain bandwidth of approximately 3KHz — a commonly used technique. Compensating the current-mode converter requires somewhat of a different approach. Since the output stage contains only a single pole, in theory closing the loop will produce a stable system with no additional compensation. In practice, however, it has been shown that subharmonic oscillation will result from excess gain at half the switching frequency ([5]).

Therefore, a pole-zero combination has been placed in the feedback loop to reduce high frequency gain and allow the output capacitor (low ESR) to roll off loop gain to 0dB at 3KHz.

Fig. 13 - Push-pull forward converter with (A) current-mode control and (B) voltage mode control.



(A) UC1846 current-mode controlled regulator



(B) UC1525A voltage mode controller

While not demonstrated in Figure 13, fixed frequency current-mode converters are known to be unstable above 50% duty cycle without some form of slope compensation (4-6). By injecting a small current from the sawtooth oscillator into the positive terminal of the current sense amplifier, slope compensation is accomplished, and the converter can be operated in excess of 50% duty cycle.

An alternate, but just as effective, scheme would be to inject the signal into the negative terminal of the error amplifier.

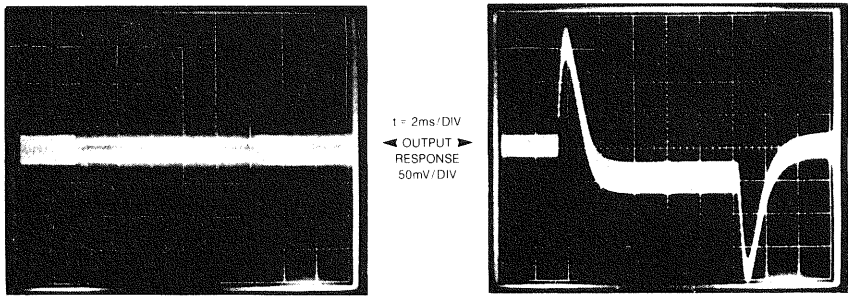
As may be seen, a similar parts count for both supplies was encountered. Topologically, using the SG1525A shutdown terminal provided only a crude current limit in contrast to the UC1846. Furthermore, internal double pulse suppression circuitry of the UC1846 gave an added level of protection against core saturation — important if your regulator is prone to subharmonic oscillations. Since both regulators were over-designed to withstand a short circuit on the output with resultant high peak currents, the shutdown-restart mode of the UC1846 was not used.

It should be pointed out at this time that one of the main features of a current-mode converter of this type is its ability to be paralleled with similar units. By disabling the oscillator and error amplifiers (C_T grounded, +E/A to V_{REF}, -E/A grounded) of one or more slave modules, and connecting SYNC and COMP pins of the slave(s) respectively, the outputs may be connected together to provide a modular approach to power supply design.

Starting with Figure 14, a comparison of line and load step responses is made between the two converters. As a result of the feed-forward effect of the current-mode converter, response to a step input change shows more than an order of magnitude improvement (Figure 14a) when compared to the conventional converter (Figure 14b). Although not as pronounced, response to a step load change leaves the UC1846 converter (Figure 15) with a clear advantage in output response — 40mV as compared to 70mV for the SG1525A.

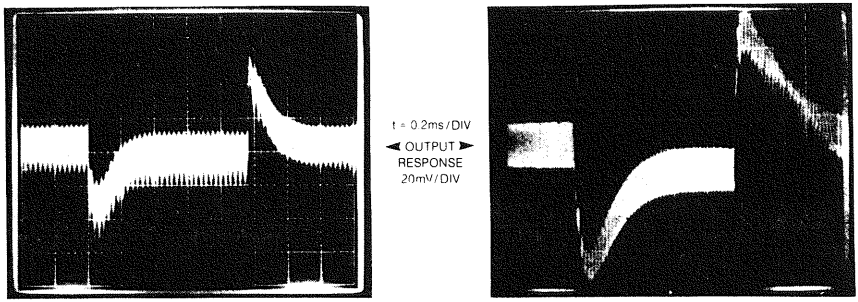
Virtually all conventional push-pull converters are prone to flux imbalance caused by mismatched storage delays, etc., in the output stage. Figure 16 shows both converters operating with the same power stage. No effort was made to match output devices. As may be seen, there is little noticeable difference between switch currents of the UC1846. However, the SG1525A — with identical output transistors — shows phase B driving the core close to saturation with 50% more current than phase A.

Fig. 14 - Response to a step input change of 25 to 35V by (A) UC1846 and (B) SG1525A converters.



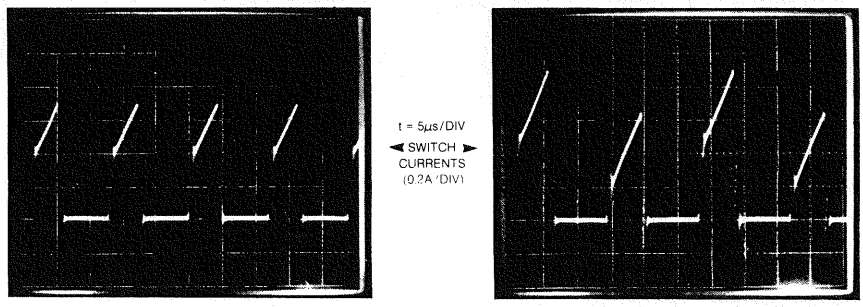
(A) (B)

Fig. 15 - Responsive to a step load change of 1 amp by (A) UC1846 and (B) UC1525A converters.



(A) (B)

Fig. 16 - Switch currents showing flux imbalance in (A) UC1846 and (B) SG 1525A converters.



(A) (B)

CONCLUSION

Rarely do new design techniques evolve that can promise as much as current-mode control for the power supply engineer. We have shown this to be a simple technique easily extended from present converter topologies, that will increase dynamic performance and provide a higher degree of reliability while permitting new approaches to modular design. Until recently, current-mode converters could not compete with the economics of conventional converters designed with I.C. controllers. Now, with the UC1846 designed specifically for this task, current-mode control can provide all of the above performance advantages on a cost competitive basis.

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NOTE - Paper written by B. HOLLAND, UNITRODE Co.

DESIGNING WITH THE L296 MONOLITHIC POWER SWITCHING REGULATOR

by G. Gattavari

A cost-effective replacement for costly hybrids, the SGS L296 Power Switching Regulator delivers 4A at an output voltage of 5.1V to 40V and includes many popular supply features. This comprehensive application guide explains how the device operates and how it is used. Typical application circuits are also presented.

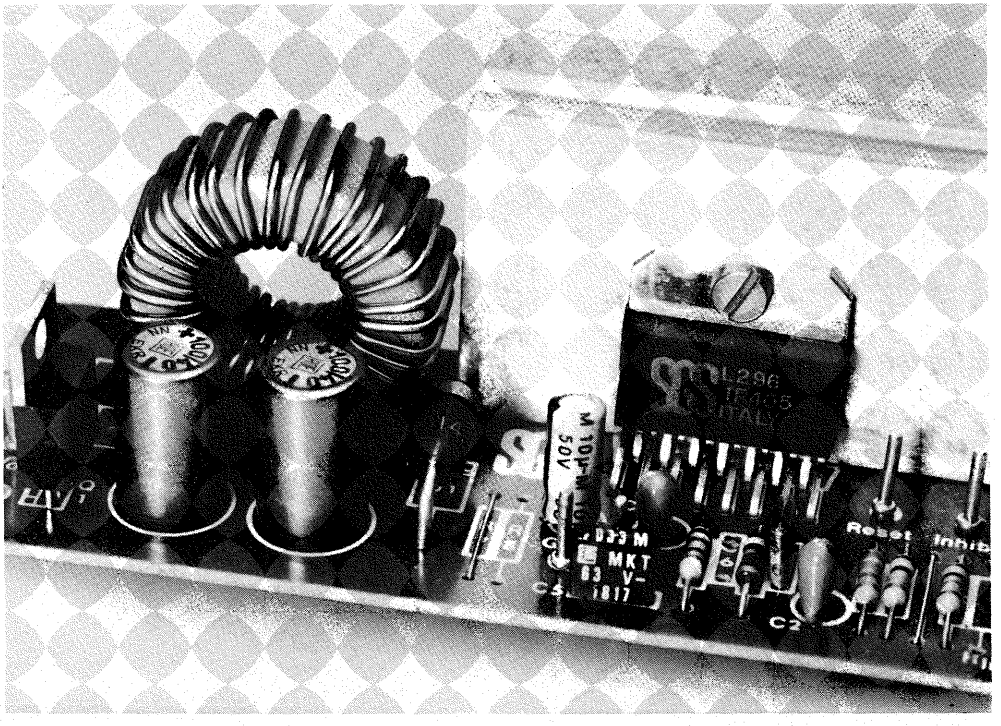


TABLE OF CONTENTS

The SGS L296 is the first monolithic switching regulator in plastic package which includes the power section. Moreover, the circuit includes all the functions which make it specially suited for microprocessor supply.

Before the introduction of L296, which realizes the step down configuration, this function was implemented with discrete power components driven by integrated PWM regulator circuits (giving a maximum output current of 300 to 400 mA) or with hybrid circuits. Both of these solutions are characterized by a low efficiency of the power transistor. For this reason it is generally necessary to operate at frequencies in the 20kHz to 40 kHz range. Of the two alternatives discrete solutions are usually less expensive because they do not include as many functions as the L296.

With the new L296 regulator the driving problem of the power control stage has been eliminated. Besides a higher overall efficiency, it is therefore also possible to operate directly at frequencies as high as 100 kHz. At 200 kHz the device still operates (further reducing the cost of the L and C external components) when a reduction of a few percent in efficiency is acceptable.

The device delivers a maximum current of 4A to the load, at an output voltage adjustable from 5.1 to 40V; the maximum operating input voltage is 46V. The high voltage and the high current capabilities of the device are a result of the special technology used and the special care taken in designing the power transistor. Essential requirements for a good power transistor are high gain and high current levels, low saturation voltage and good second breakdown robustness. To achieve high gain at high current levels, the power transistor has to be designed to maximize the emitter's perimeter/area ratio.

In the L296 power transistor, realized with a high voltage (50V) process, current densities in the magnitude order of 10 mA/Mil^2 are achieved.

In its most complete configuration, in which all the available functions are being used, a significant reduction of the external component count is achieved compared with discrete component solution.

The L296 is mounted in a MULTIWATT® plastic package with 15 pins, minimizing the cost per watt and allowing a low thermal resistance of 3°C/W between junction and package and of 35°C/W between junction and ambient. This thermal resistance (including the contact resistance) is comparable to that of the more costly metal TO-3 packages.

THE STEP-DOWN CONFIGURATION

Fig. 1 shows the simplified block diagram of the circuit realizing the step-down configuration. This circuit operates as follows: Q1 acts as a switch at the frequency f and the ON and OFF times are suitably controlled by the pulse width modulator circuit. When Q1 is saturated, energy is absorbed from the input which is transferred to the output through L. The emitter voltage of Q1, V_E, is Vi-Vsat when Q is ON and $-V_F$ (with V_F the forward voltage across the D diode as indicated) when Q1 is OFF. During this second phase the current circulates again through L and D. Consequently a rectangular-shaped voltage appears on the emitter of Q1 and this is then filtered by the L-C-D network and converted into a continuous mean value across the capacitor C and therefore across the load. The current through L consists of a continuous component, I_{LOAD}, and a triangular-shaped component superimposed on it, ΔI_L, due to the voltage across L.

Fig. 1 — The basic step-down switching regulator configuration.

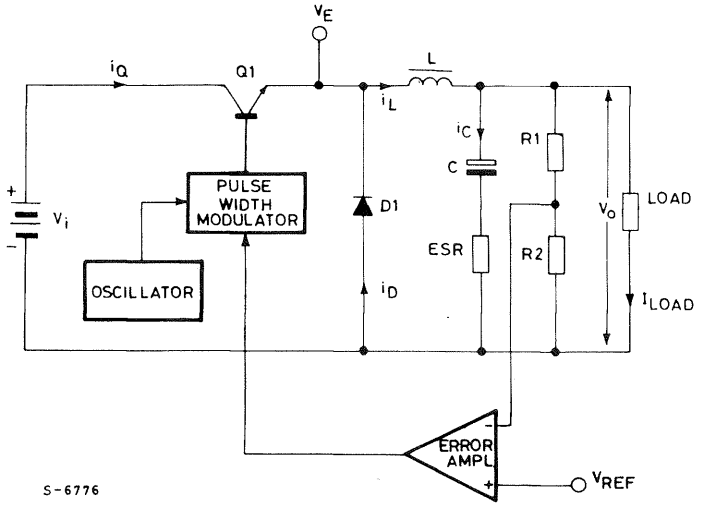


Fig. 2 – Principal circuit waveforms of the fig. 1 circuit.

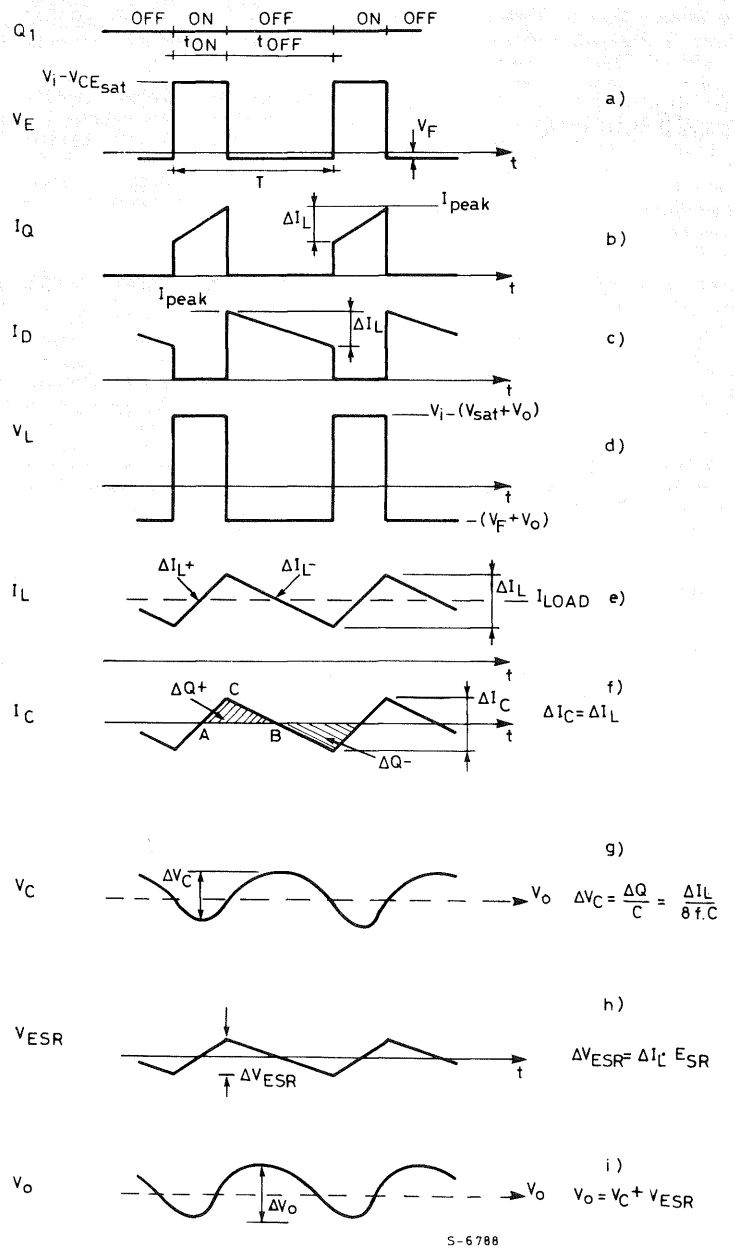


Fig. 2 shows the behaviour of the most significant waveforms, in different points of the circuit, which help to understand better the operation of the power section of the switching regulator. For the sake of simplicity, the series resistance of the coil has been neglected. Fig. 2a shows the behaviour of the emitter voltage (which is practically the voltage across the recirculation diode), where the power saturation and the forward V_F drop across the diode era taken into account.

The ON and OFF times are established by the following expression:

$$V_o = (V_i - V_{sat}) \frac{T_{ON}}{T_{ON} + T_{OFF}}$$

Fig. 2b shows the current across the switching transistor. The current shape is trapezoidal and the operation is in continuous mode. At this stage, the phenomena due to the catch diode, that we consider as dynamically ideal, are neglected. Fig. 2c shows the current circulating in the recirculation diode. The sum of the currents circulating in the power and in the diode is the current circulating in the coil as shown in fig. 2e. In balanced conditions the ΔI_L^+ current increase occuring during T_{ON} has to be equal to the ΔI_L^- decrease occurring during T_{OFF}. The mean value of I_L corresponds to the charge current.

The current ripple is given by the following formula:

$$\Delta I_L^+ = \Delta I_L^- = \frac{(V_i - V_{sat}) - V_o}{L} T_{ON} = \frac{V_o + V_F}{L} T_{OFF}$$

It is a good rule to respect to $I_{oMIN} \geqslant I_L/2$ relationship, that implies good operation in continuous mode. When this is not done, the regulator starts operating in discontinuous mode. This operation is still safe but variations of the switching frequency may occur and the output regulation decreases.

Fig. 2d shows the behaviour of the voltage across coil L. In balanced conditions, the mean value of the voltage across the coil is zero. Fig. 2f shows the current flowing through the capacitor, which is the difference between I_L and I_{LOAD}.

In balanced conditions, the mean current is equal to zero, and $\Delta I_C = \Delta I_L$. The current I_C through the capacitor gives rise to the voltage ripple.
This ripple consists of two components: a capacitive component, ΔV_C, and a resistive component, ΔV_{ESR}, due to the ESR equivalent series resistance of the capacitor. Fig. 2g shows the capacitive component ΔV_C of the voltage ripple, which is the integral of a triangular-shaped current as a function of time. Moreover, it should be observed that v_C (t) is in quadrature with i_C(t) and therefore with the voltage V_{ESR}. The quantity of charge ΔQ^+ supplied to the capacitor is given by the area enclosed by the ABC triangle in fig. 2f:

$$\Delta Q = \frac{1}{2} \cdot \frac{T}{2} \cdot \frac{\Delta I_L}{2}$$

which therefore gives:

$$\Delta V_C = \frac{Q}{C} = \frac{\Delta I_L}{8fc}$$

Fig. 2h shows the voltage ripple V_{ESR} due to the resistive component of the capacitor. This component is v_{ESR} (t) = i_C (t) • ESR. Fig. 2i shows the overall ripple V_o, which is the sum of the two previous components. As the frequency increases (> 20 kHz), which is required to reduce both the cost and the sizes of L and C, the V_{ESR} component becomes dominant. Often it is necessary to use capacitors with greater capacitance (or more capacitors connected in parallel to limit the value of ESR within the required level.

We will now examine the stepdown configuration in more detail, referring to fig. 1 and taking the behaviour shown in fig. 2 into account.

Starting from the initial conditions, where Q = ON, $v_C = V_o$ and $i_L = i_D = 0$, using Kirckoff second principle we may write the following expression:

$V_i = v_L + v_C$ (Vsat is neglected against V_i).

$$V_i = L \frac{di_L}{dt} + v_C = L \frac{di_L}{dt} + V_o \qquad (1)$$

which gives:

$$\frac{di_L}{dt} = \frac{(V_i - V_o)}{L} \qquad (2)$$

The current through the inductance is given by:

$$I_L = \frac{(V_i - V_o)}{L} t \qquad (3)$$

When V_i, V_o, and L are constant, I_L varies linearly with t. Therefore, it follows that:

$$\Delta I_L^+ = \frac{(V_i - V_o)\, T_{ON}}{L} \qquad (4)$$

When Q is OFF the current through the coil has reached its maximum value, I_{peak} and because it cannot vary instantaneously, the voltage across the coil is inverted and the diode D becomes forward biased to allow the recirculation of the current through the load.

When Q switches OFF, the following situation is present:

$v_C(t) = V_o$, i_L (t) = i_D (t) = I_{peak}

And the equation associated to the following loop may be written:

$$V_F + L \frac{di_L}{dt} + v_C = 0 \qquad (5)$$

where:

$v_C = V_o$

$$\frac{di_L}{dt} = -(V_F + V_o)/L \qquad (6)$$

It follows therefore that:

$$i_L(t) = -\frac{V_F + V_o}{L} t \qquad (7)$$

The negative sign may be interpretated with the fact that the current is now decreasing. Assuming that V_F may be neglected against V_o, during the OFF time the following behaviour occurs:

$$I_L = \frac{V_o}{L} t \qquad (8)$$

therefore:

$$\Delta I_L^- = \frac{V_o}{L} T_{OFF} \qquad (9)$$

But, because

$\Delta I_L^+ = \Delta I_L^-$ if follows that :

$$\frac{(V_i - V_o)\, T_{ON}}{L} = \frac{V_o\ T_{OFF}}{L}$$

which allows us to calculate V_o:

$$V_o = V_i \frac{T_{ON}}{T_{ON} + T_{OFF}} = V_i \frac{T_{ON}}{T} \qquad (10)$$

where T is the switching period.

Expression (10) links the output voltage V_o to the input voltage V_i and to the duty cycle. The relationship between the currents is the following:

$$I_{iDC} = I_{oDC} \cdot \frac{T_{ON}}{T}$$

EFFICIENCY

The system efficiency is expressed by the following formula:

$$\eta\% = \frac{P_o}{P_i} 100$$

where $P_o = V_o I_o$ (with $I_o = I_{LOAD}$)

is the output power to the load and P_i is the input power absorbed by the system. P_i is given by P_o, plus all the other system losses. The expression of the efficiency becomes therefore the following :

$$\eta = \frac{P_o}{P_o + P_{sat} + P_D + P_L + P_q + p_{sw}} \qquad (12)$$

DC LOSSES

P_{sat}: saturation losses of the power transistor Q. These losses increase as V_i decreases.

$$P_{sat} = V_{sat} \cdot I_o \frac{T_{ON}}{T} = V_{sat}\ I_o \frac{V_o}{V_i} \qquad (13)$$

where $\frac{T_{ON}}{T} = \frac{V_o}{V_i}$ and V_{sat} is the power transistor saturation at current I_o.

P_D: losses due to the recirculation diode. These losses increase as V_i increases, as in this case the ON time of the diode is greater.

$$P_D = V_F\ I_o \frac{V_i - V_o}{V_i} = V_F\ I_o\ (1 - \frac{V_o}{V_i}) \qquad (14)$$

where V_F is the forward voltage of the recirculation diode at current I_o.

P_L: losses due to the series resistance R_S of the coil

$$P_L = R_S\ I_o^2 \qquad (15)$$

P_q: losses due to the stand-by current and to the power driving current:

$$P_q = V_i\ I'_{3q} + V_i\ I''_{3q} \frac{T_{ON}}{T} \qquad (16)$$

where being:

$\frac{T_{ON}}{T} = \frac{V_o}{V_i}$ it follows that :

$P_q = V_i\ I'_{3q} + V_o\ I''_{3q}$ in which :

$I'_{3q} = I_{3q}$ at 0% duty cycle

$I''_{3q} = I_{3q\,(100\%\,d.c.)} - I_{3q\,(0\%\,d.c.)}$

SWITCHING LOSSES

p_{sw}: switching losses of the power transistor:

$$p_{sw} = V_i\ I_o \frac{t_r + t_f}{2T}$$

The switching losses of the recirculation diode are

neglected (which are anyway negligible) as it is assumed that diode is used with recovery time much smaller than the rise time of the power transistor.

We can neglect losses in the coil (it is assumed that ΔI_L is very small compared to I_o) and in the output capacitor, which is assumed to show a low ESR.

Calculation of the inductance value, L

Calculating T_{ON} and T_{OFF} through (4) and (9) respectively it follows that:

$$T_{ON} = \frac{\Delta I_L^+ \cdot L}{V_i - V_o} \qquad T_{OFF} = \frac{\Delta I_L^- \cdot L}{V_o}$$

But because:

$$T_{ON} + T_{OFF} = T \quad \text{and} \quad \Delta I_L^+ = \Delta I_L^- = \Delta I_L,$$

it follows that:

$$\frac{\Delta I_L \cdot L}{V_i - V_o} + \frac{\Delta I_L \cdot L}{V_o} = T$$

Calculating L, the previous relation becomes:

$$L = \frac{(V_i - V_o)\ V_o}{V_i\ \Delta I_L} T \qquad (18)$$

Fixing the current ripple in the coil required by the design (for instance 30% of I_o), and introducing the frequency instead of the period, it follows that:

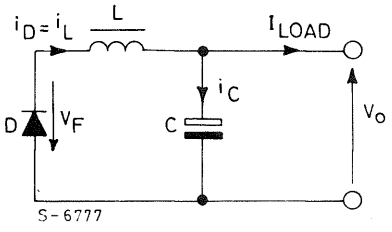
$$L = \frac{(V_i - V_o) V_o}{V_i \cdot 0.3 \cdot I_o \cdot f}$$ where L is in Henry and f in Hz

Calculation of the output capacitor C

From the output node in fig. 3 it may be seen that the current through the output capacitor is given by:

$$i_c(t) = i_L(t) - I_o$$

Fig. 3 – Equivalent circuit showing recirculation when Q_1 is turned off.



From the behaviour shown in fig. 2 it may be calculated that the charge current of the output capacitor, within a period, is $\Delta I_L/4$, which is supplied for a time T/2. It follows therefore that:

$$\Delta V_C = \frac{\Delta I_L}{4C}\frac{T}{2} = \frac{\Delta I_L\, T}{8C} = \frac{\Delta I_L}{8fC} \qquad (19)$$

but, remembering expression (4):

$$\Delta I_L^+ = \frac{(V_i - V_o)\ T_{ON}}{L} \quad \text{and} \quad T_{ON} = \frac{V_o}{V_i} T$$

therefore equation (19) becomes:

$$\Delta V_C = \frac{(V_i - V_o)\ V_o}{8\, V_i\, f^2\, L\, C}$$

Finally, calculating C it follows that:

$$C = \frac{(V_i - V_o)\ V_o}{8\, V_i\, \Delta V_C\, f^2\, L} \qquad (20)$$

where: L is in Henrys
C is in Farads
f is in Hz

Finally, the following expression should be true:

$$ESR_{max} = \frac{\Delta V_{Cmax}}{\Delta I_L} \qquad (21)$$

It may happen that to satisfy relation (21) a capacitance value much greater than the value calculated through (20) must be used.

TRANSIENT RESPONSE

Sudden variations of the load current give rise to overvoltages and undervoltages on the output voltage. Since $i_c = C\,(dv_C/dt)$ (22), where $dv_C = \Delta V_o$, the instantaneous variation of the load current ΔI_o is supplied during the transient by the output capacitor. During the transient, also current through the coil tends to change its value.
Moreover, the following is true:

$$v_L = L \frac{di_L}{dt} \qquad (23) \quad \text{where} \quad di_L = \Delta I_o.$$

$v_L = V_i - V_o$ for a load increase

$v_L = V_o$ for a load decrease

Calculating dt from (22) and (23) and equalizing, it follows that:

$$L \frac{di_L}{v_L} = C \frac{dv_c}{i_c}$$

Calculating dv_c and equalizing it to ΔV_o, it follows that:

$$\Delta V_o = \frac{L \Delta I_o^2}{C(V_i - V_o)} \quad (24) \quad \text{for} + \Delta I_o$$

$$\Delta V_o = \frac{L \Delta I_o^2}{C V_o} \quad (25) \quad \text{for} - \Delta I_o$$

From these two expressions the dependence of overshoots and undershoots on the L and C values may be observed. To minimize ΔV_o it is therefore necessary to reduce the inductance value L and to increase the capacitance value C. Should other auxiliary functions be required in the circuit like reset or crowbar protections and very variable loads may be present, it is worthwhile to take special care for minimizing these overshoots, which could cause spurious operation of the crowbar, and the undershoot, which could trigger the reset function.

DEVICE DESCRIPTION

Fig. 4 shows the package in which the device is mounted and the pin function assignments.
The internal structure of the device is shown in fig. 5. Each block will now be examined.

Power supply

The device is provided with an internal stabilized power supply that, besides supplying the reference voltage of 5.1V for the whole system, also supplied the internal analog blocks.
Special features of the voltage reference are its accuracy, temperature stability and high line rejection. Through zener-zap trimming, the voltage is within ± 2% limits.

Fig. 4 – Pin assignments of the L296.

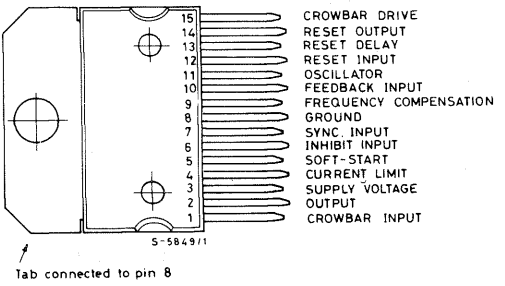
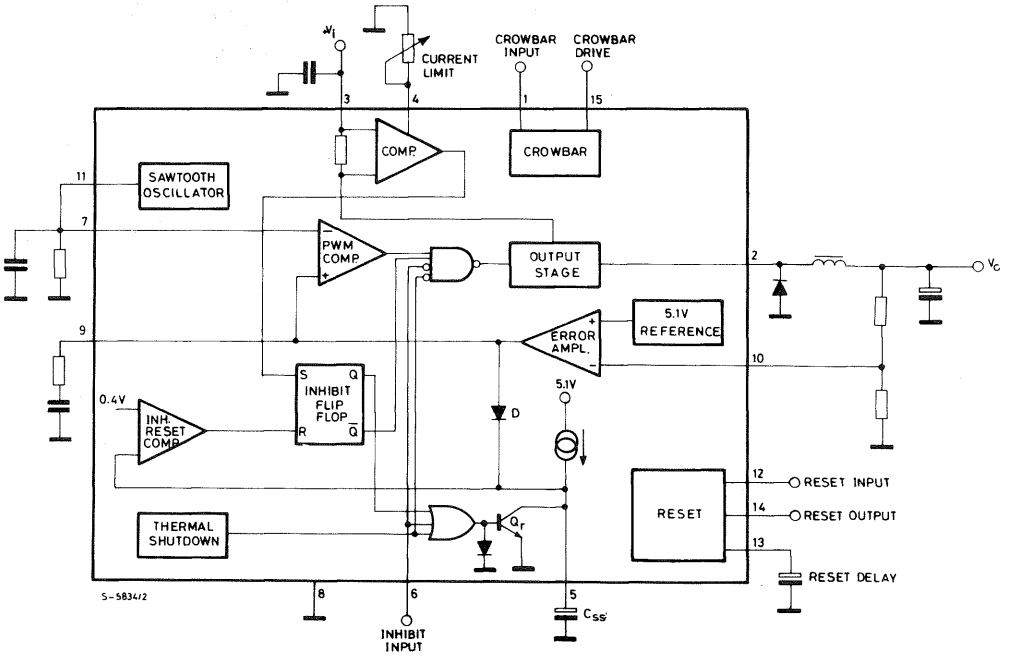


Fig. 5 – Block diagram of the L296. In addition to the basic regulation loop the device includes functions such as reset, crowbar and current limiting.



OSCILLATOR

The oscillator block generates the saw-tooth waveform that sets the switching frequency of the system. This signal, compared with the output voltage of the error amplifier, generates the PWM signal to be sent to the power output stage. The saw-tooth, whose amplitude is between 1.2V and 3.2V, is generated by charging rapidly the C_{osc} capacitor which then discharges across the R_{osc} resistance. As shown in fig. 6, the oscillator is realized by a comparator (with grounded compatible input) with hysteresis whose thresholds are 1.2V and 3.2V respectively. The C_{osc} capacitor and the R_{osc} resistance are connected to the non-inverting input of the comparator which set the oscillating frequency is fixed. When the voltage on pin 11 is less than 3.2V, the switch S_1 is closed and the current generator charges the C_{osc} capacitor rapidly; in this phase S_2 is also closed. As soon as 3.2V is reached the comparator output drives S_2 open (therefore opening S_1, too); the inverting input voltage is reduced to about 1.2V and the capacitor starts to discharge itself across the R_{osc} resistor (the I_{bias} effect is neglected). When the voltage reaches 1.2V, S_2 and S_1 close again and a new cycle starts. The generated waveform is shown in fig. 7.

To achieve a good accuracy of the switching frequency it is essential to have a charging time of the capacitor which is much smaller than the discharging time. In this way, the oscillation frequency only depends on the external components C_{osc} and R_{osc}. For this reason the capacitor charging current (when S_1 is ON) is typically around 10 mA. For example, with a 2.2 nF capacitor to switch from 1.2V to 3.2V about 400 ns is required, which is negligible compared to the 10 μs period that occurs when the operation is performed at 100 kHz. The diagrams shown in fig. 8 allow the calculation of the R_{osc} value (R_1 in fig. 8) with C_{osc} as a parameter (C_3 in fig. 8) when the oscillation frequency required for operation has been previously fixed.

Fig. 7a – Oscillator waveform at pin 11 with f = 100 KHz (R_{osc} = 4.3 KΩ, C_{osc} = 2.2 nF)

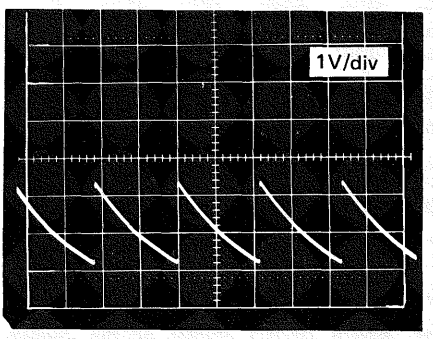


Fig. 7b – Oscillator waveform at pin 11 with f = 50 KHz (R_{osc} = 9.1 KΩ, C_{osc} = 2.2 nF)

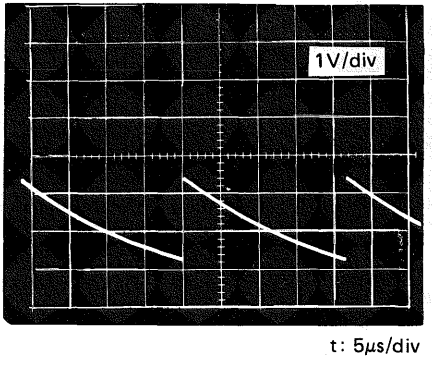


Fig. 6 – Internal schematic of the oscillator

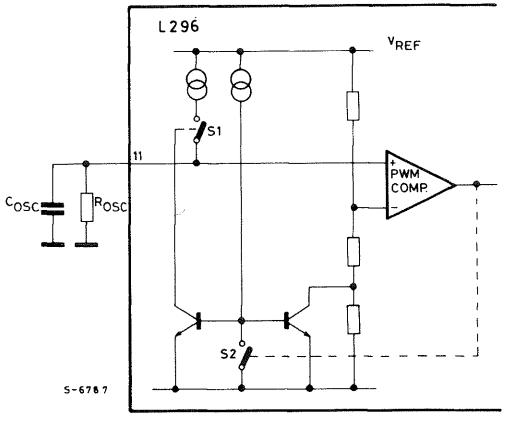


Fig. 8 - Nomogram for the choice of oscillator components.

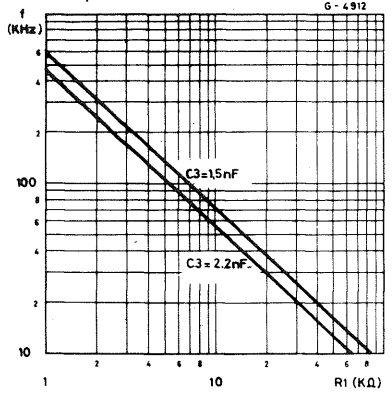


Fig. 8 shows two suggested values for the C_{osc} capacitance. Excessively low capacitance value may give rise to an inaccuracy of the upper threshold

due to the switching delays of the comparator. This inaccuracy in caused by an excessively short rise time of the voltage. A capacitance value too high gives rise to a charging time which is too long compared to the discharging time. An additional inaccuracy cause would be therefore present for the switching frequency, now due to spread of the charge current.

The oscillation frequency is given by the following formula:

$$f_{osc} = \frac{1}{R_{osc}\ C_{osc}} \qquad (26)$$

PWM (see fig. 9)

The PWM signal is generated on the comparator output; the triangular-shaped waveform and the continuous signal coming from the output of the transconductance error amplifier are sent to its inputs. The PWM signal is then transferred to the driving stage of the output power transistor.

SOFT START (see fig. 9)

Soft start is an essential function for correct start-up, to prevent stresses and possible breakdown from occurring in the power transistor and to obtain a monotonically increasing output voltage.
In particular, the L296, as it does not have any duty cycle limitation and due to the type of current limitation does not allow the output to be forced to a steady state without the aid of the soft-start facility. Soft-start operates at the start-up of the system, after the inhibit has been activated, after an intervention of the current limitation and after the intervention of the thermal protection.

The soft-start function is realized through a capacitor connected to pin 5 which is charged at constant current ($\cong 100\mu A$) up to a value of about V_{REF}. During the charging time, through PNP transistor Q58, the voltage on pin 9 is forced to increase with the same rising speed as on pin 5. Starting from the discharged capacitor condition (pin 5 voltage = 0V) the power transistor is in the OFF condition, as the voltage on pin 9 is smaller than the minimum level of the ramp voltage. As the capacitor is charged, the PWM signal begins to be generated as soon as the error amplifier output voltage crosses the ramp; the power stage starts to switch with steadily increasing duty cycle. This behaviour is shown in fig. 10. As soon as the steady condition is reached the duty cycle sets itself to the right value due to the effect of the feedback network while the soft-start capacitor completes its charging to a value very close to V_{REF}.

The soft-start effect is determined, apart from the switch-on time, when the current limitation operates, due to either an overload or a short circuit, to keep the mean value of the current absorbed by the power supply low.
Moreover from fig. 11 it may be observed that since the voltage on pin 9 can decrease under the minimum ramp level and increase over the maximum level no limitations have been provided on the duty cycle, which therefore may vary between 0 and 100%.

Fig. 9 – Partial internal schematic showing PWM and soft start blocks.

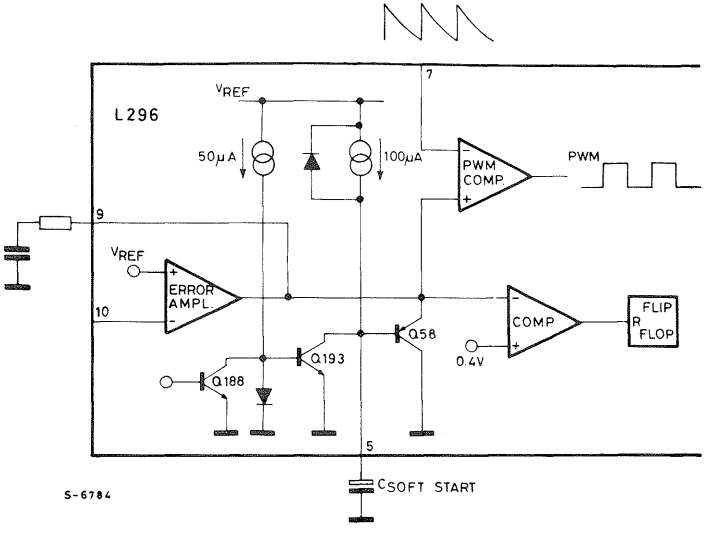


Fig. 10 – Soft start waveforms. When power is applied, or after an inhibit, the L296's output current rises slowly under control of the soft start circuit.

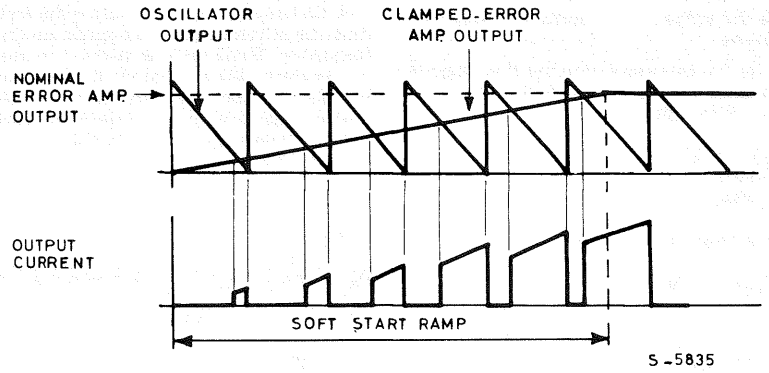
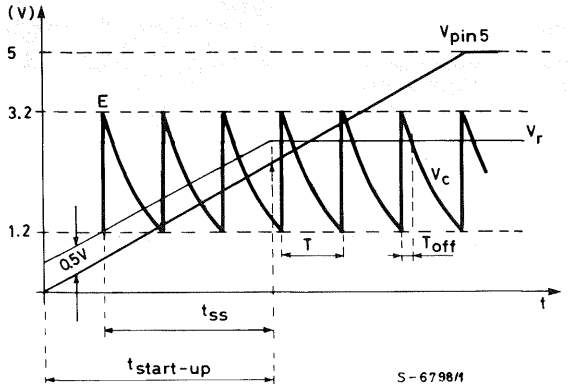


Fig. 11 – Waveform for calculation of duty cycle and soft start time.



CALCULATING THE DUTY CYCLE AND SOFT-START TIME

Assume, for simplicity, that the rising edge of the ramp is instantaneous; V_r is the output voltage of the error amplifier and V_c the ramp voltage (see fig. 11). The PWM comparator block switches when $V_r = V_c$; therefore:

$$V_r = V_c = E\, e^{-\frac{t}{R_{osc}\, C_{osc}}}$$

Consequently:

$$t = R_{osc}\, C_{osc}\, \ln \frac{E}{V_r}$$

The time obtained from this expression is the T_{OFF} time of the power transistor. The duty cycle d is given by:

$$d = \frac{T_{ON}}{T} = \frac{T - R_{osc}\, C_{osc}\, \ln \frac{E}{V_r}}{T} = \quad (27)$$

$$= 1 - \ln \frac{E}{V_r} = \frac{V_o}{V_i}$$

Consequently, starting with the capacitor discharged, the output of the regulator will be at the nominal level when the voltage at the terminal of the capacitor (which is charged by a constant current) has reached $V_r - 0.5V$.

$$t_{start\text{-}up} = \frac{C_{ss}\ (V_r - 0.5V)}{I_{5so}}$$

where C_{ss} is the soft-start capacitor and I_{5so} is the charging current.

Considering as the soft-start time the time required for the soft-start capacitor to charge from (1.2V-0.5V) to $V_r - 0.5V$, gives:

$$t_{ss} = \frac{C_{ss}\ (V_r - 1.2)}{I_{sso}} \qquad (28)$$

substituting V_r from (27) gives:

$$V_r = E\ e^{-\left(1 - \frac{V_o}{V_i}\right)}$$

substituting into (28) gives:

$$t_{ss} = \frac{C_{ss}}{I_{sso}} \left(E\ e^{\left(\frac{V_o}{V_i} - 1\right)} - 1.2 \right)$$

SYNCHRONIZATION

The synchronization function is available on pin 7, this function allows the device to be switched at an externally generated frequency (leaving pin 11 open), or to mutually synchronize several devices, using one of them as master and the others as slave (Fig. 12).

This allows several devices to be operated at the same frequency, avoiding undesirable intermodulation phenomena. The number of mutually synchronizable devices is obviously much greater than the three devices shown in the figure. It is anyway difficult to establish an exact maximum number of devices, as it depends on different conditions.

The first consideration concerns the accuracy which must be achieved and maintained on the oscillation frequency. Since the bias current on pin 7 is an output current, the sum of all the bias currents must be much smaller than the capacitor discharge current in close proximity to the lower discharge threshold. Therefore, assuming $C_{osc} = 2.2$ nF and $R_{osc} = 4.3\ K\Omega$, it follows that:

$$\frac{1.2V}{4.3\ K\Omega} = 280\mu A$$

Assuming that a 10% variation may be accepted, it follows therefore that the number of synchronizable devices is given by:

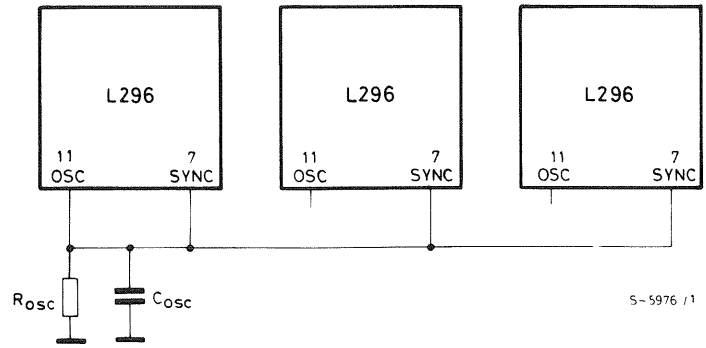
$$N = \frac{28\ \mu A}{I_{bias\ max}}$$

This means that if the overall I_{bias} is too high it may modify the discharging time of the capacitor.

The second consideration concerns the layout design.
In the presence of a great number of devices to be synchronized, the lenght of the paths may become significant and therefore the distributed inductance introduced along the paths may begin to modify the triangular shaped waveform, particularly the rising edge which is very steep. This effect would affect the devices that are physically located more distant from the master device.

The amplitude of the saw-tooth to be externally connected must be within 0.5V and 3.5V, values also representing the maximum swing of the error amplifier output.

Fig. 12 – In multiple supplies several L296's can be synchronized as shown here.



CURRENT LIMITATION

The current limitation function has been realized in a rather innovative way to avoid overload condition during the short circuit operation. In fact, while for all the other devices a constant current limitation is implemented by acting on the duty cycle (therefore, in short circuit conditions an output current is equal to the maximum limitation current), the new control approach allows operation in short circuit conditions with a mean current much smaller than the allowed 4A value. Operation of the current limiter will now be described.
Refer to the block diagram, fig. 13.

The current which is delivered from the output transistor to the load flows through the current sensing resistor R_S. When the voltage drop on R_S is equal to the offset voltage of the current comparator, the comparator generates a set pulse for the flip-flop, with a delay of about 1 μsec. The purpose of this delay is to avoid triggering of the protection circuit on the current peak that occurs during the recirculation phase. Therefore, the output $\overline{Q}$ goes low and the power stage is immediately switched off, while the output Q goes high and acts directly on the soft-start capacitor discharging the soft-start capacitor at a costant current (about 50 μA).

When the voltage on pin 5 reaches 0.4V the comparator triggers, supplying a reset pulse to the flip-flop; from now on, the power stage is enable and the soft-start phase starts again. When the limitation cause, either overload or short circuit, is still present the cycle repeats again. The waveform of the output current on pin 2 is shown in fig. 14.

From fig. 14 it may be observed how this current limitation technique allows the short circuit operation with a very low output current value.

It is possible to reduce the maximum current value by acting on pin 4. On this pin a voltage of about 3.3V is present; by connecting a resistance a constant current, given by 3.3/R, is sent to ground. This current reduces the offset voltage of the current comparator, therefore anticipating its triggering threshold.

Fig. 13 – Partial schematic showing the current limiter circuit.

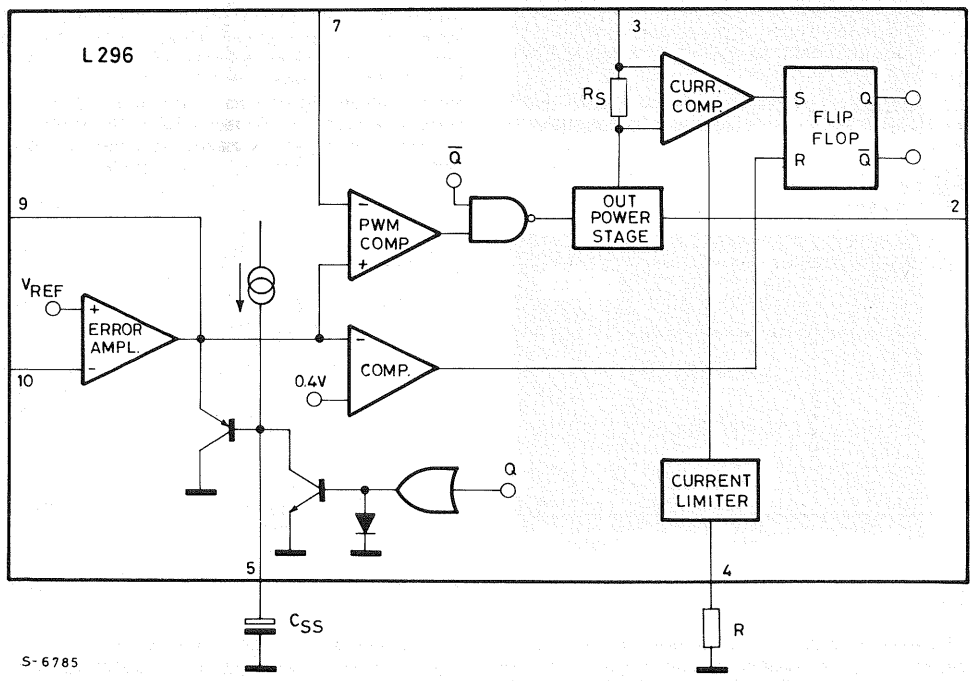


Fig. 14a – Current limiter waveforms.

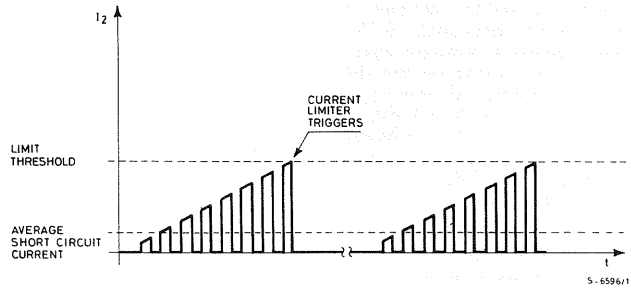
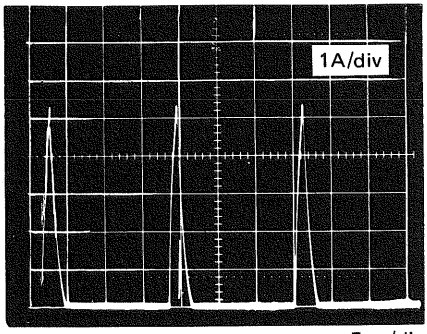
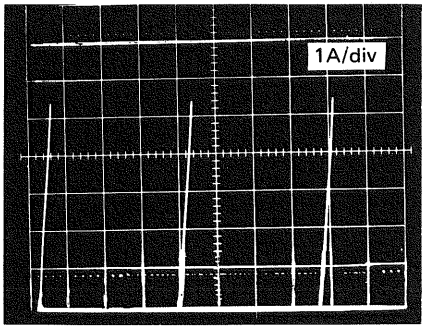


Fig. 14b – Load current in short circuit conditions ($V_i = 40v$, $L = 300\ \mu H$, $f = 100\ KHz$)



t: 5ms/div

Fig. 14c – Current at pin 2 when the output is short circuited.



t: 5ms/div

RESET

The reset function is of great importance when the device is used to supply microprocessors, logic devices, and so on. This function differentiates the SGS L296 device from all previous devices. The block diagram of the function is shown in fig. 15. A reset signal is generated when the output voltage is within the limits required to supply the microprocessor correctly.

The reset function is realized through the use of 3 pins: the reset input pin 12, the reset delay pin 13 and the reset output pin 14. When the voltage on pin 12 is smaller than 5V the comparator output is high and the reset capacitor is not charged because the transistor Q is satured and the voltage on pin 14 is at low level, since Q2 is saturated, too. When the voltage on pin 12 goes above 5V, the transistor Q switches OFF and the capacitor can start to charge through a current generator of about 100 μA. When the voltage on pin 13 goes above 4.5V the output of the related comparator switches low and the pin 14 goes high. As the output consists of an open collector transistor, a pull-up external resistance is required. In contrast, when the reset input voltage goes below 5V, less a hysteresis voltage of about 100 mV, the comparator triggers again and instantaneously sets the voltage on pin 14 low, therefore forcing to saturation the Q1 transistor, that starts the rapid discharge of the capacitor. Obviously, the reset delay is again present when the voltage on pin 13 is allowed to go under 4.5V.

To achieve switching operations without uncertainties the two comparators have been provided with an hysteresis of about 100 mV. In every operating condition the reset switching is guaranteed with a minimum reset input of 4.75V, the value required for correct operation of the microprocessor even in the presence of the minimum V_{REF} value.

Normally pin 12 is used connected to pin 10. When it is connected to the output, the function may be more properly called "reset"; on the other hand, when it is connected through resistive divider, to the input voltage, the function is called "power fail". Fig. 16 and fig. 17 show the two possible usages.

The "power-fail" function is used to predict, with a given advance, the drop of the regulator output voltage, due to main failures, which is enough to save the data being processed into protected memory areas. Fig. 18 summarises the reset function operation.

Fig. 15 — Partial schematic showing reset circuit.

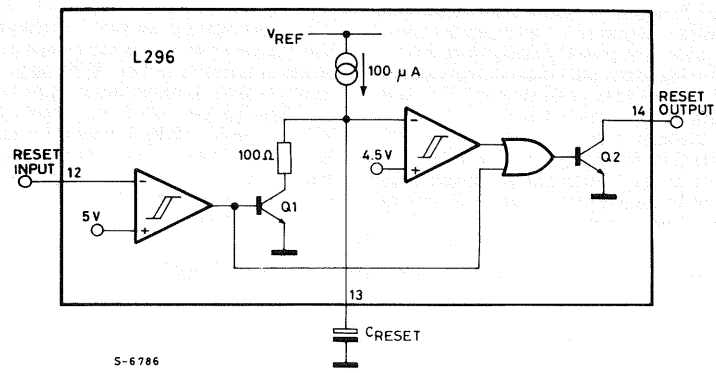


Fig. 16 — For power - on reset the reset block is connected as shown here.

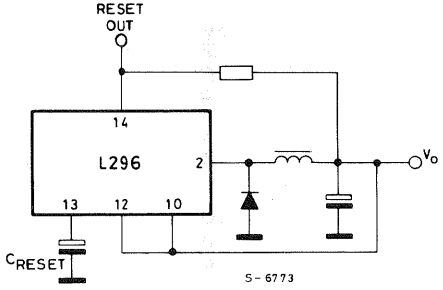


Fig. 17 — To obtain a power fail signal, the reset block is connected like this.

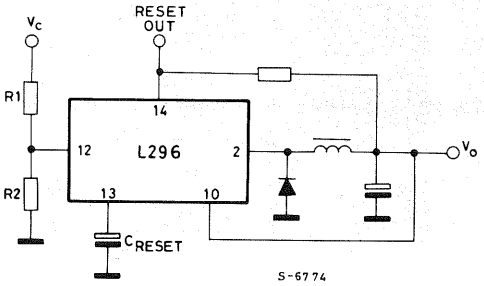
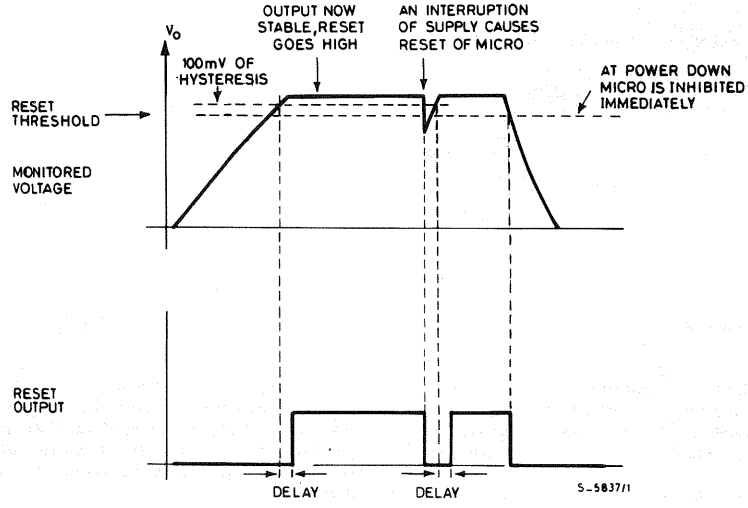


Fig. 18 — Waveform of the reset circuit.



CROWBAR

This protection function is realized by a completely independent block, using pin 1 as input and pin 15 as output. It is used to prevent dangerous overvoltages from occurring when the output exceeds 20% of rated value. Pin 15 is able to output a 100 mA current to be sent to the gate of a SCR which, triggering, short circuits either output or the input. When connected to the input, as the SCR is triggered a fuse in series connected to power supply is blown and to bring the system back to operation manual intervention is requested. Figs. 19, 20 and 21 show the different configurations.

When the voltage on pin 1 exceeds by about 20% the V_{REF} value the output stage is activated, which sends a current to the SCR gate, after a delay of about 5 μsec to make the system insensitive to low-duration spikes. When activated, the output stage delivers about 100mA; when not activated, it drains about 5 mA and shows a low impedance to the SCR gate to avoid uncorrect triggering due to random noise. If the crowbar function is not used connect pin 1 to ground.

Fig. 19 – Connection of crowbar circuit at output for 5.1V output applications.

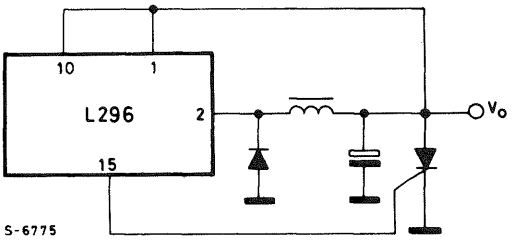


Fig. 20 – Connection of crowbar circuit at output for output voltages above 5.1V.

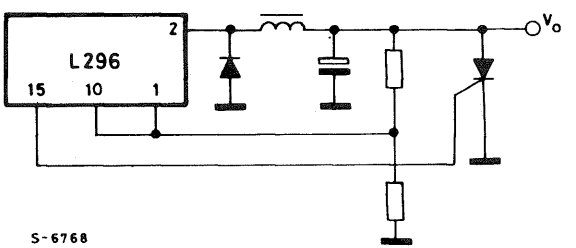
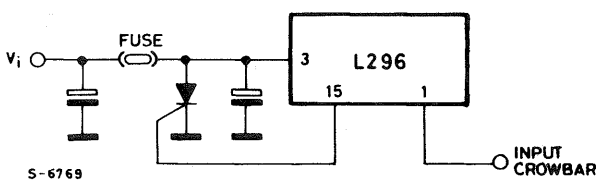


Fig. 21 – Connection of crowbar circuit to protect input. When triggered, the SCR blows the fuse.



INHIBIT

The inhibit input (pin 6) is TTL compatible and is activated when the voltage exceeds 2V and deactivated when the voltage goes under 0.8V. As may be seen in the block diagram, the inhibit acts on the power transistor, instantaneously switching it off and also acts on the soft-start, discharging its capacitor. When the function is unused, pin 6 must be grounded.

THERMAL PROTECTION

The thermal protection function operates when the junction temperature reaches 150°C; it acts directly on the power stage, immediately switching it off, and on the soft-start capacitor, discharging it. The thermal protection is provided with hysteresis and, therefore, after an intervention has occurred, it is necessary to wait for the junction temperature to decrease of about 30°C below the intervention threshold.

APPLICATIONS

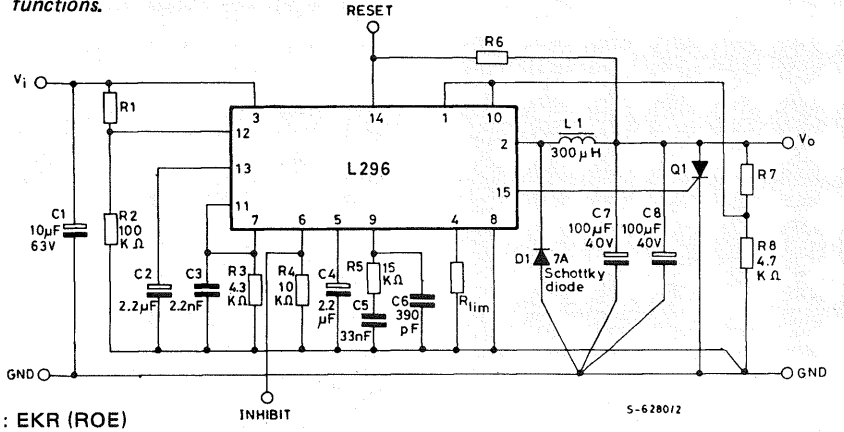
Though the L296 is designed for step-down regulator configurations it may be used in a variety of other applications. We will now examine these possibilities and show how the capabilities of the device may be extended.

In fig. 22 the complete typical application is shown, where all the functions available on the device are being used. This circuit delivers to the load a maximum current of 4A and a voltage which is established by the voltage divider constituted by R_7 and R_8 resistances. The following table is helpful for a quick calculation of some standard output voltages:

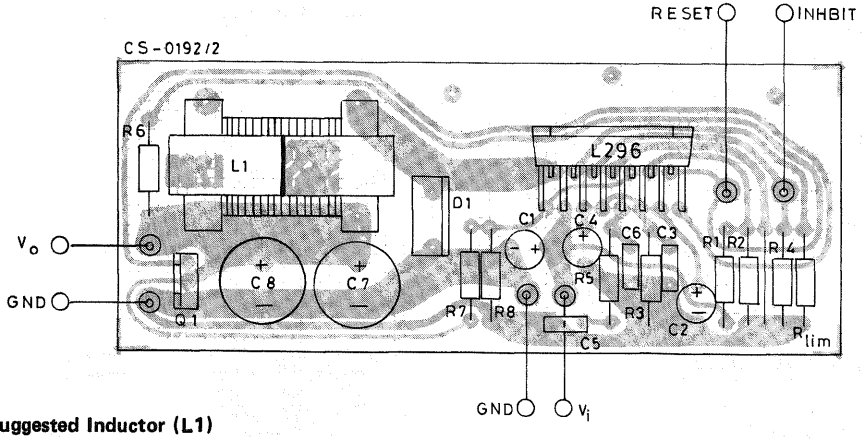
Resistor value for standard output voltages		
V_o	R_8	R_7
12V	4.7 kΩ	6.2 kΩ
15V	4.7 kΩ	9.1 kΩ
18V	4.7 kΩ	12 kΩ
24V	4.7 kΩ	18 kΩ

To obtain $V_o = V_{REF}$ the pin 10 is directly connected to the output, therefore eliminating both R_7 and R_8. The switching frequency is 100 kHz.

Fig. 22 – Schematic, PCB layout and suggested component values for the evaluation circuit used to characterize the L296. This is a typical stepdown application which exercises all the device's functions.



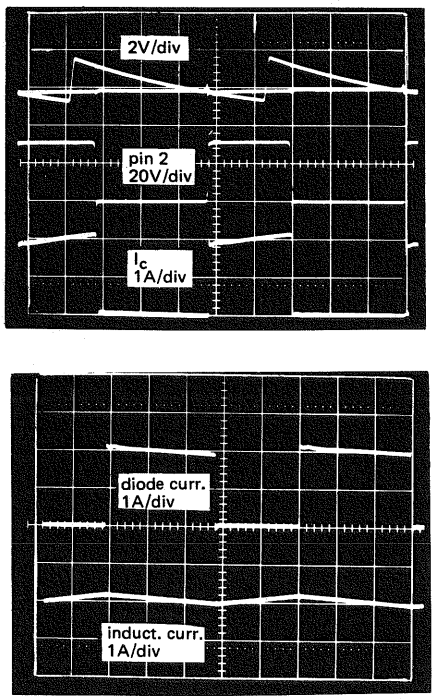
C7, C8 : EKR (ROE)



Suggested Inductor (L1)

Core Type	No Turns	Wire Gauge	Air Gap
Magnetics 58930 - A2MPP	43	1.0 mm.	–
Thomson GUP 20x16x7	65	0.8 mm.	1 mm.
Siemens EC 35/17/10 (B6633& - G0500 - X127)	40	2 x 0.8 mm.	–
VOGT 250 µH Toroidal coil, part number 5730501800			

Fig. 23 – Oscilloscope photographs showing main waveforms of the figure 22 circuit.



The oscilloscope photographs of the main waveforms are shown in fig. 23. The output voltage ripple ΔV_o depends on the current ripple in the coil and on the performance of the output capacitor at the switching frequency (100 kHz). A capacitor suitable for this kind of application must have a low ESR and be able to accept a high current ripple, at the working frequency. For this application the Roederstein EKR series capacitors have been selected, designed for high frequency applications (>200 kHz) and manufactured to show low ESR value and to accept high current ripples. To minimize the effects of ESR, two 100 μF/40V capacitors have been connected in parallel. The behaviour of the impedance as a function of frequency is shown in fig. 24.

Also the selection of the catch diode requires special care. The best choice is a Schottky diode which minimizes the losses because of its smaller forward voltage drop and greater switching frequency rate. A possible limitation comes from the backward voltage, that generally reaches 40V max.
When the full input voltage range of the device is required in this application it is possible to use super fast diodes with 35 to 50 ns rated recovery time, where no more problems on the backward voltage occur (on the other hand, they show a greater forward voltage). The use of slower diodes, with trr = 100 ns or more is not recommended; The photographs in fig. 25 show the effects on the power current and on the voltage on pin 2, due to the diodes showing different speeds. Diodes showing trr greater than 35-50 ns will reduce the overall efficiency of the system, increasing the power dissipated by the device.

The third component requiring care is the inductor. Fig. 22a shows the part numbers of some types used for testing. Besides having the required inductance value, the coil has to show a very high saturation current.
Therefore, a correct dimensioning requires a saturation current above the maximum value of I_{2L}, the current limit threshold.

To achieve high saturation with ferrite cores an air gap between the two core halves must be provided; the air gap causes a leakage flux which is radiated in the surrounding space. To better limit this phenomenon "pot cores" may be used, whose geometry is such to better limit the flux radiated to the outside.
Using toroidal cores, for instance of Magnetic 58930-A2 moly-permalloy kind, both the requirements of high saturation and low leakage flux are satisfied. The saturation is softer that the saturation shown by the ferrite materials. The air gap is not concentrated in one area, but is finely distributed along the whole core; this gives the low leakage flux value.

Careful selection of the external components therefore allows the realization of a power supply system whose benefits are significant when compared to a system with the same performance but realized with the linear technique.

Fig. 24 – Typical impedance/frequency curves for EKR capacitors.

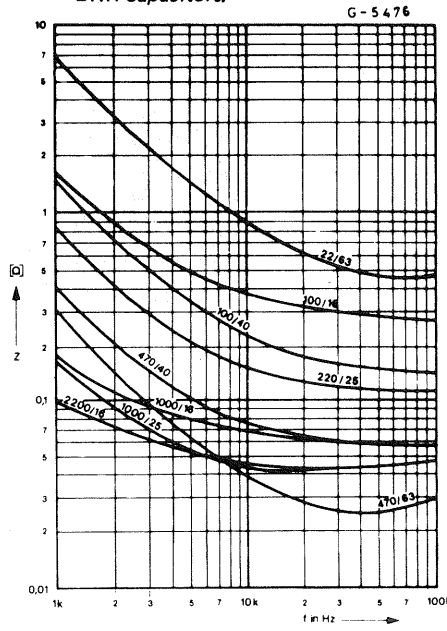
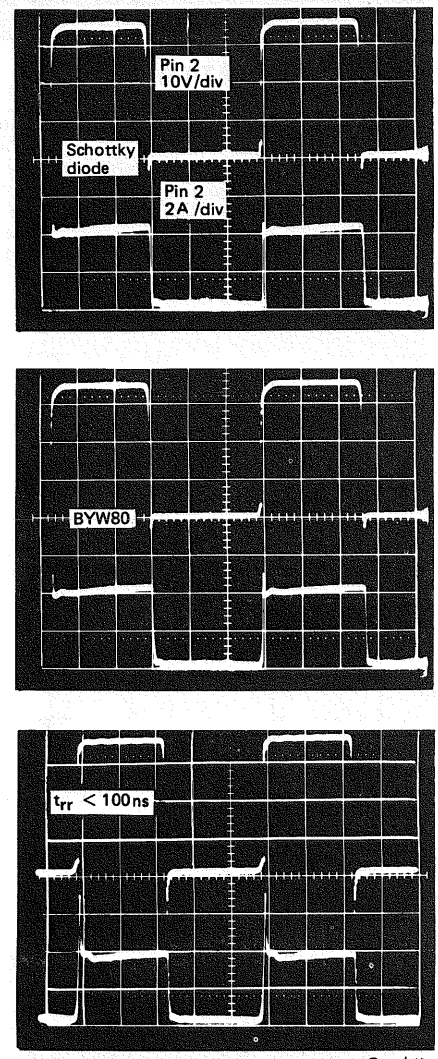


Fig. 25 – Oscilloscope photographs showing the waveforms obtained with diodes having different t_{rr} values.



t: 2μs/div

SWITCHING vs LINEAR

Switching regulators are more efficient than linear types so the transformer and heatsink can be smaller anc cheaper. But how much can you gain ?

We can estimate the savings by comparing equivalent linear and switching regulators. For example, suppose that we want a 4A/5V supply.

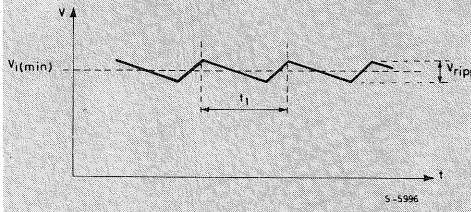
Linear

For a good linear regulator the minimum dropout will be a least 5V at 4A. The minimum input voltage is given by:

$$V_{i\,min} = V_o + V_{drop} + \frac{1}{2} V_{ripple}$$

where:

$$V_{ripple} \simeq \frac{I_o\ t_1}{C} = \frac{4 \times 8 \times 10^{-3}}{10 \times 10^{-3}} = 3.2V$$



(a good approximation is 8 ms for t_1 at mains frequency of 50Hz and 10.000 μF for C, the filter capacitor after the bridge). Therefore $V_{i\,min} \cong 10.6V$. Since operation must be guaranteed even when the mains voltage falls 20% , the nominal voltage on load at the terminals of the regulator must be:

$$V_{nom} = \frac{V_{i\,min}}{0.8} = \frac{10.6}{0.8} = 13.25V$$

To allow even a small margin we have to choose:

$$V_{nom} = 14V$$

The power that the series element must dissipate is therefore:

$$P_d = (V_{nom} - V_o)\ I_o = 36\,W$$

and a heatsink will be necessary with a thermal resistance of:

$$R_{th\ heats.} = 0.8\,°C/W$$

and the transformer must supply a power of:

$$P_{diss} = 14 \times 4 = 56W$$

It must therefore be dimensioned for:

$$P_D = \frac{56}{0.9} = 62VA$$

Switching (L296)

Assuming the same nominal voltage (14V), the L296 data sheet indicates that the power dissipated in this case is only 7W. And this power is dissipated in two elements; the L296 itself and the recirculation diode.

It follows that the trasnformer must be roughly 30VA and the heatsink thermal resistance about 11 °C/W.

	Linear	Switching
Transformer	62 VA	30 VA
Heatsink	0.8 °C/W	11 °C/W

This comparison shows that the L296 switching regulator allows a saving of roughly 50% on the cost of the transformer and an impressive 80-90% on the cost of the heatsink. Considering also the extra functions integrated by the L296 the total cost of active and passive components is roughly the same for both types.

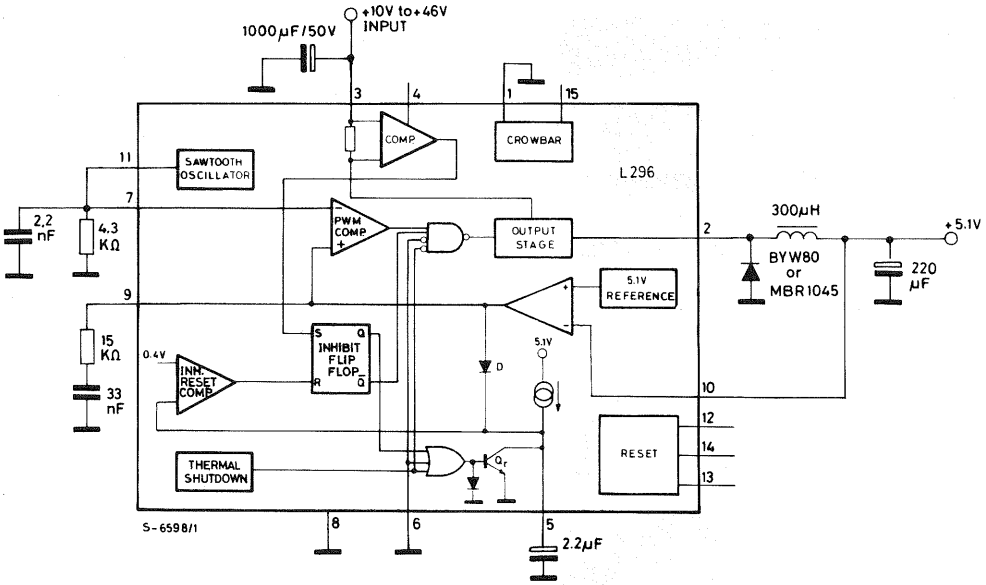
Finally, it is important to note that a lower power dissipation means that the ambient temperature in the regulator enclosure can be lower - particularly when the circuit is enclosed in a box - with all the advantages cooler operation brings.

If for some reason it is necessary to use higher supply voltages the switching technique, and hence the L296, becomes even more advantageous.

LOW COST APPLICATION AND PREREGULATOR

Fig. 26 shows the low cost application of a 4A and V_o = 5.1V power supply. A minimum amount of essential external components is required, which are necessary for correct operation. It is impossible to save other components, specially the soft-start capacitor. Without soft-start, the system cannot reach the steady state and there is also a serious risk of damaging the device.

Fig. 26 – A minimal component count 5.1V/4A supply.



This application is very well suited not only as a low-cost power supply, but also as pre-regulator for post-regulators distributed in different circuit points, or even on different boards (Fig. 27). The post-regulators may be selected among the low-drop types, like L4805 and L387 for example, still obtaining a high efficiency, combined with an excellent regulation. The use of L387 device allows us to use also the reset function, useful to power a micropocessor.

POWER SUPPLY COMPLETE WITH TRANSFORMER

Fig. 28 shows a power supply complete of transformer, bridge and filter, with regulation on the output voltage from 5.1V to 15V.

As already stated above, the output capacitors have to show some speciale features, like low ESR and high current ripple, to obtain low voltage ripple values and high reliability. The input filter capacitors must not be neglected because they have to show excellent features, too, having to supply a pulsed current, required by the device at the switching frequency. The current ripple is rather high, greater than the load current. For this application, two parallel connected 3300 µF/50V EYF (ROE) capacitors have been used.

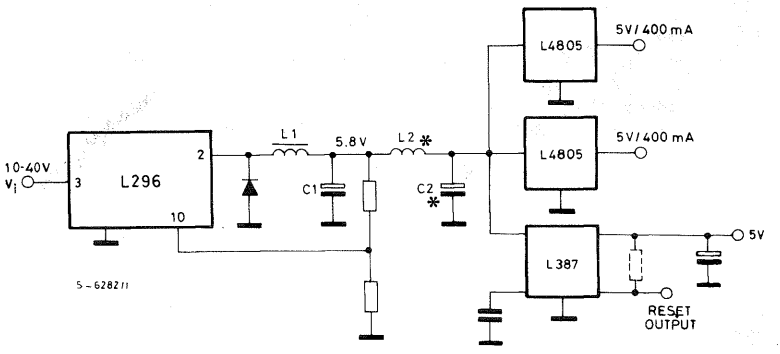
POWER SUPPLY WITH MAINS SWITCHING PREREGULATOR

When it is desirable to eliminate the 50/60 Hz transformer – in portable or volume-limited equipment – a mains preregulator can be added to reduce the input voltage to a level acceptable for the L296.

In this case the pre-regulator circuit is connected to the primary of the transformer which now operates at the switching frequency and is therefore smaller and lighter.

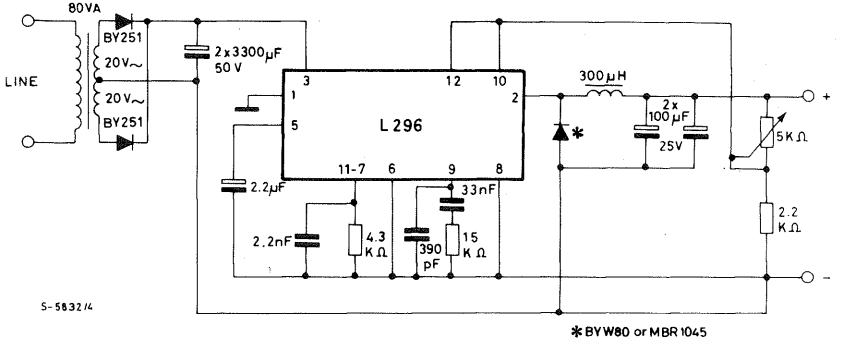
Using a UC3840 which includes the feed-forward function it is possible to compensate mains variation within wide limits. The secondary voltage is therefore only affected by load variations. Using one or more L296s as postregulators, feedback to the primary is no longer necessary, reduces the complexity and cost of the transformer which needs only a single secondary winding.
Fig. 28A shows a multi-output supply with a mains preregulator.

Fig. 27 – The L296 may also be used as a preregulator in distributed supply systems.



* L2 and C2 are necessary to reduce the switching frequency spikes.

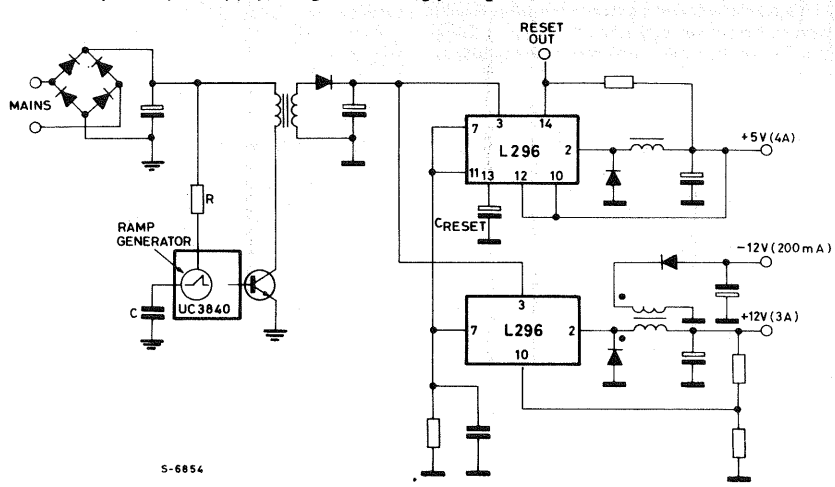
Fig. 28 – A typical variable supply showing the mains transformer.



* BYW80 or MBR1045

V_o = 5.1 to 15V
I_o = 4A max. (min. load current = 100 mA)
ripple ⩽ 20 mV
load regulation (1A to 4A) = 10 mV (V_o = 5.1V)
line regulation (220V ± 15% and to I_o = 3A) = 15 mV (V_o = 5.1V)

Fig. 28A – A multiple output supply using a switching preregulator rather than a mains transformer.



POWER SUPPLY WITH 0 – 30V ADJUSTABLE VOLTAGE

When output voltages lower than 5V are required, the circuit shown in fig. 29 may be used.

Calibration is performed by grounding the P1 slider. Acting on P2, the current which flows through the 10 kΩ resistor is fixed at approximately 2.5mA to obtain an output voltage of 30V. The equivalent circuit is shown in fig. 30.

Acting now on the slider of P1, the current flowing through the divider may be varied. The new equivalent circuit is shown in fig. 31.

Reducing the current flowing, also the voltage drop across the 10kΩ resistance is reduced, together with V_o. When the current reaches zero, it follows that $V_o = V_{REF}$. When the voltage on the slider of P1 exceeds V_{REF}, the current start to flow in opposite direction and V_o begins to decrease below 5V.

When $I_1 \times 10K\Omega = V_{REF}$ it follows that $V_o = 0$.

Fig. 29 – Variable 0–30 V supply illustrating how output voltages below 5.1V are obtained.

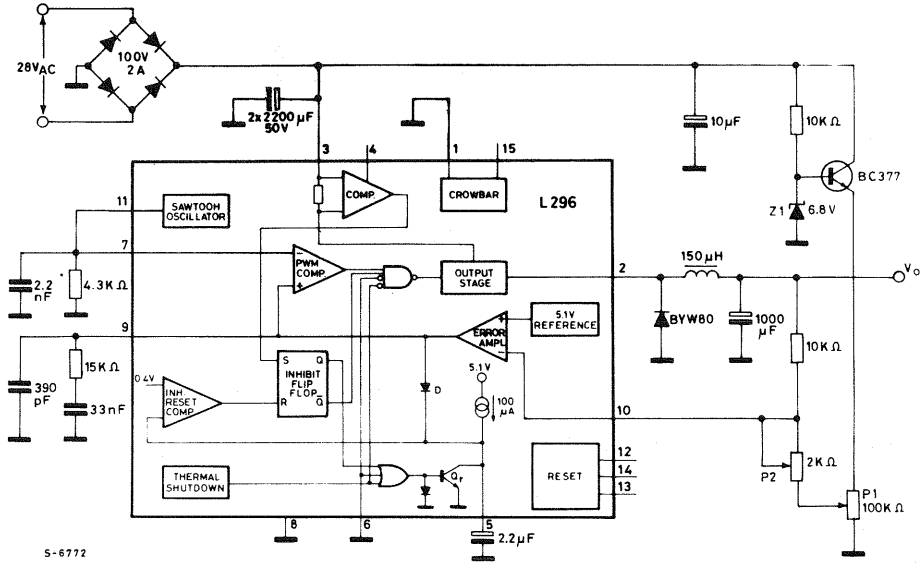


Fig. 30 – When setting up the figure 29 circuit the slider of P1 is grounded, giving the equivalent circuit shown here, and P2 adjusted to give an output voltage of 30 V.

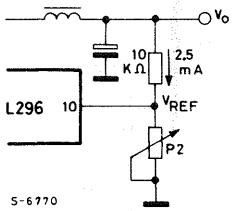
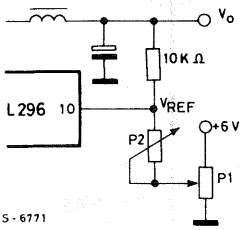


Fig. 31 – Partial schematic showing output voltage adjustment of figure 29.

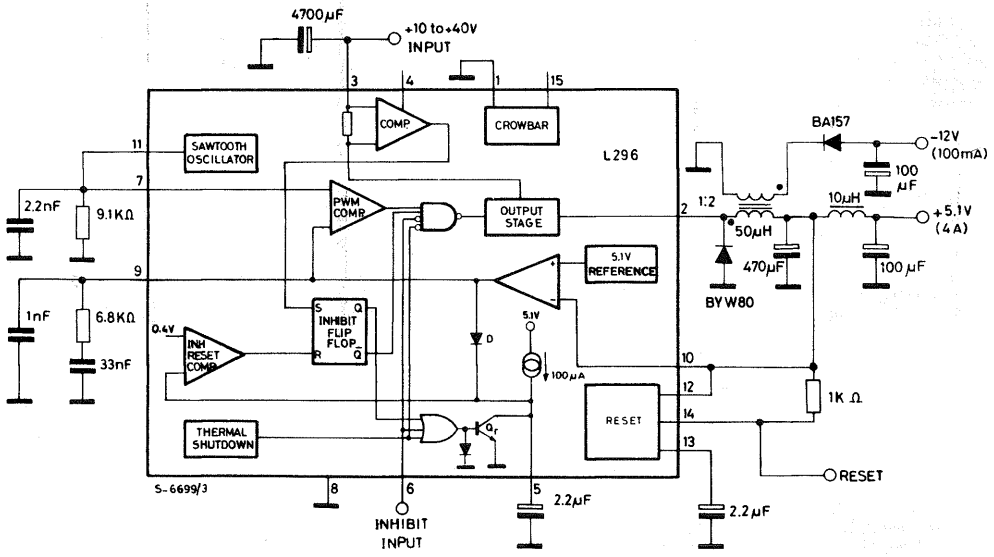


DUAL OUTPUT REGULATOR

The application shown in fig. 32 is specially interesting because it provides two output voltages. The first voltage, the main one, is directly controlled by the feedback circuit. The second voltage is obtained through an auxiliary winding.

It often happens, when microprocessors, logic devices etc., have to be power supplied, that a main 5V output and an auxiliary + 12V or – 12V output are required, the latter with lower current requirements (100 ÷ 200 mA) and a stabilization level not excessively high. As the auxiliary power supply is obtained through a completely separated winding, it is possible to obtain either a positive or negative voltage (compared to the main voltage or also a completely isolated voltage. With V_i variable between 20V and 40V, V_o = 5.1V and I_o = 2.5A, the auxiliary -12V/0.2A voltage is within a ± 2% tolerance.

Fig. 32 – Dual output regulator showing how an additional winding can be added to the inductor to generate a secondary output.



PERSONAL COMPUTER POWER SUPPLY

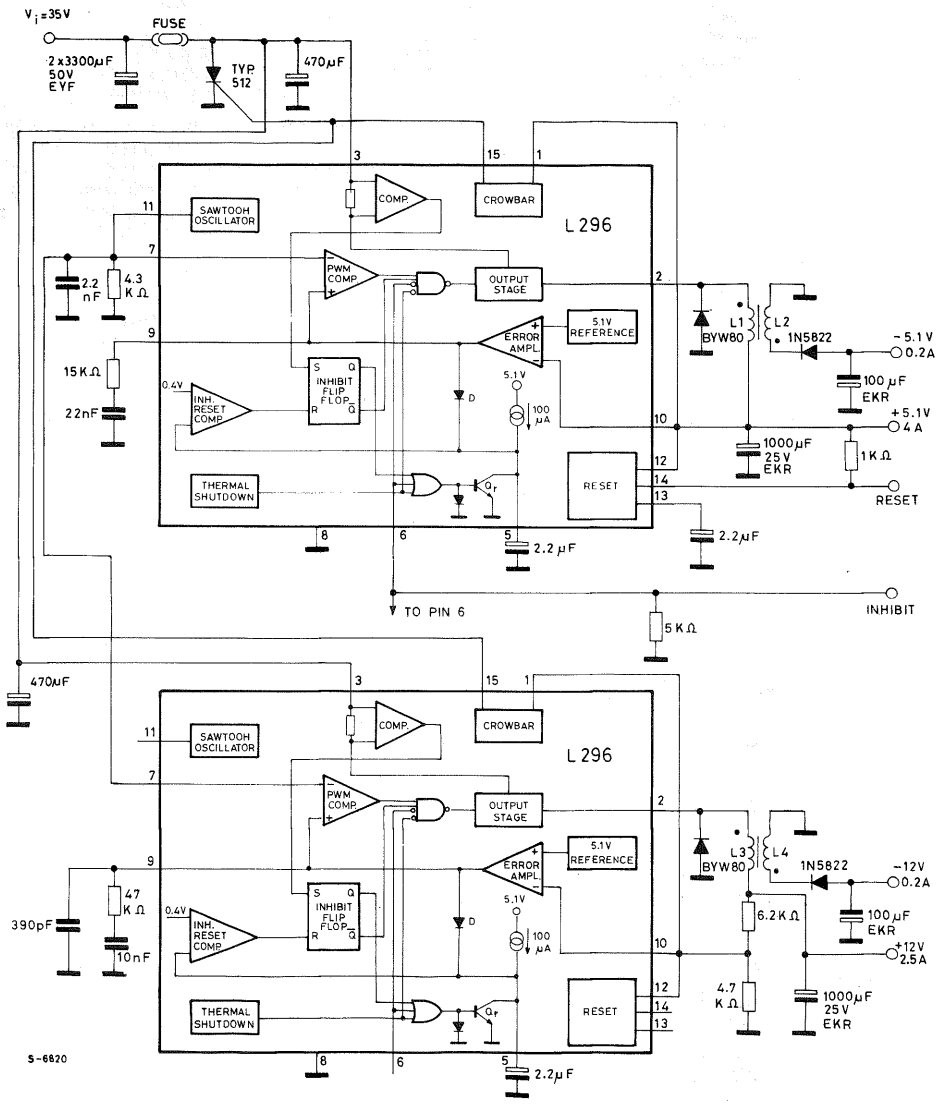
Using two mutually synchronized devices it is possible to obtain a four output power supply suitable for power a microprocessor system.

V_{01} = 5.1V/4A
V_{02} = 12V/2.5A (up to 4A)
V_{03} = –5V/0.2A
V_{04} = –12V/0.2A

The schematic diagram is shown in fig. 33. The 5V output is also provided with the reset function, that is available also for the 12V output.

The feedback is direct, no other external component is used and no calibration is therefore required. An output is obtained with the accuracy of the reference voltage (± 2%). For the 12V output, by using a resistive divider with 1% resistance an output is obtained whose spread is within ± 4%.

Fig. 33 – Microcomputer supply with 5V, -5V, 12V and -12V outputs.



The two devices are mutually synchronized not to give rise to intermodulation which could generate unpleasant noise and, at the same time, a further component saving is achieved.

The crowbar function is implemented on both 5V and 12V outputs, using a single SCR connected to the input. The latter, by discharging to ground the electrolytic filter capacitors, blows the fuse connected in series with the devices power supply. In this way, should a faulty be present on either of the main outputs, the supply is switched off for whole system.

To inhibit both the devices with a single input signal, it is possible to connect the two inhibit inputs (pin 6) together; the 5KΩ resistance is used when the inhibit input is left open. If this input is not used it must be grounded.

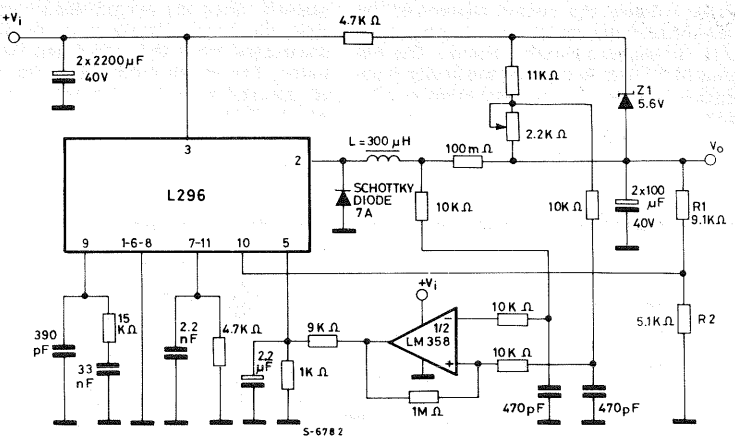
As may be noted in the diagram, to obtain the two auxiliary voltages is very simple and cost-effective.

It is suggested that the diodes are fast types (trr< 50 nsec); should slower diodes be required some more turns have to be added to the auxiliary winding.

BATTERY CHARGER

When the device has to be used as current generator it is necessary to avoid the internal current limiter is operated Fig. 34 shows the circuit realizing constant current limitation. In this way it is possible to obtain a 6V, 12V and 24V battery charger. For each of these voltages a max. current of 4A is available, which is large enough for batteries up to 40-45 Ah (for 12V type). With reference to the electric diagram through the 2KΩ potentiometer the max output current is set, while through the $R_1 - R_2$ output divider the voltage is set. (R_1 may be replaced by either a potentiometer or a 3 position switch, to directly obtain the three 6V, 12V and 24V voltages).

Fig. 34 – Battery charger circuit illustrating how the device is used to regulate the output current.



HIGHER INPUT VOLTAGE

Since a maximum input voltage of 46V (operating value) may be applied to the device the diagram shown in fig. 35 may be used when it is necessary to exceed this limit.

This system is particularly useful when operating at low output voltages. In this case a mean current I_{iDC} which has a low value when compared to I_o is obtained. In fact, since $V_o = V_i (T_{ON}/T)$ and $V_o I_o = V_i I_{iDC}$ (assuming the device has an ideal efficiency), it follows that $I_{iDC} = I_o (T_{ON}/T)$.

Assuming to be:

$V_o = 5V$ $I_o = 4A$ and $V_3 \simeq 37V$,

it follows that:

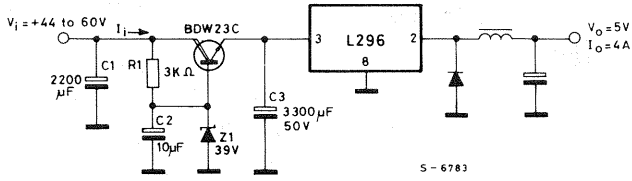
$$T_{ON}/T = V_o/V_i = \frac{5}{37} = 0.135$$

$I_{iDC} = 4 \times 0.135 = 0.54A.$

With input voltage 50V and $I_o = 4A$, the external transistor dissipates about 7W. High good efficiency is still achieved, around 74%; in the real case, considering also the device losses, an afficiency around 62% is achieved.

During output short circuits the external transistor is not overloaded because in this condition I_{iDC} reduces to values lower than 100mA. It is not possible to realize this application with series post-regulator because the efficiency would be unacceptably low.

Fig. 35 – The maximum input voltage can be raised above 46V by adding a transistor as shown here.



MOTOR CONTROL

The L296 is also suitable for use in motor controls applications. Fig. 36 shows how to use the device to drive a motor with a maximum power of about 100W and provided with a tachometer generator for a good speed control.

HIGHER CURRENT REGULATORS

It is possible to increase the output current to the load above 4A through the use of an external power transistor. Fig. 37 shows a suitable circuit. The frequency is around 40 kHz to prevent the device from loosing excessive power due to switching on the external power.

The circuits shown in fig. 38 and fig. 39 show how current limitation may be realized in two different ways: through a sensing resistor connected in series with the collector of the external power transistor or through a current transformer.

In the first case, the sensing resistor is a low value resistor able to withstand the maximum load current required. The V_{CE} of the power transistor is higher than its V_{CEsat}; when the resistor is connected in series to the collector V_{CE} is reduced; consequently since the overall dissipated power is constant, the power dissipated by the sensing resistor is subtracted from that dissipated by the power transistor. The values indicated in figs. 38 and 39 realize adjustable current limitation for load currents around 10A.

Fig. 36 – With a tacho dynamo supplying feedback the L296 can be used as a motor speed controller.

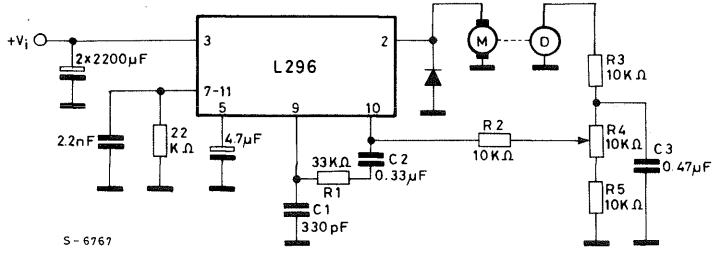


Fig. 37 – The output current may be increased by adding a power transistor as shown in this circuit.

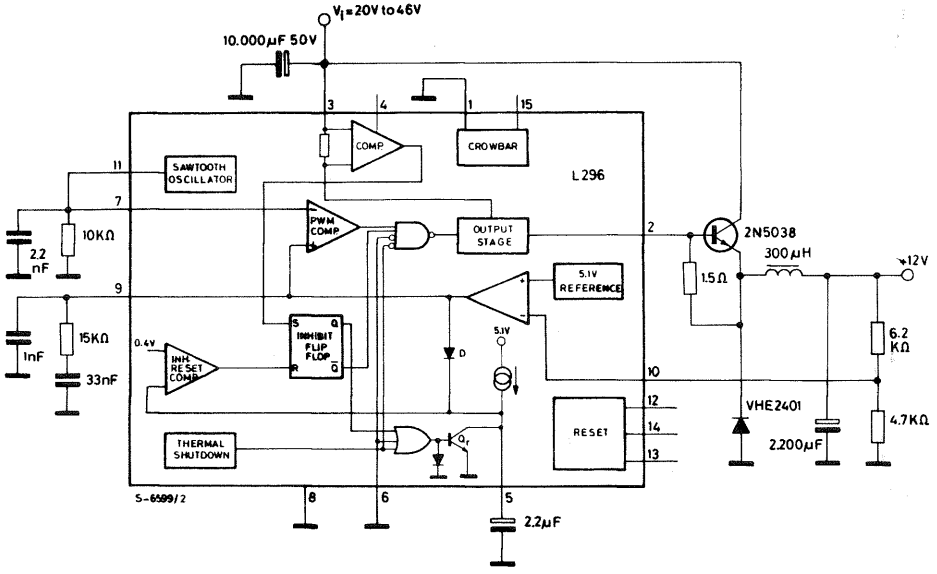


Fig. 38 – This circuit shows how current limiting for the external transistor is obtained with a sensing resistor.

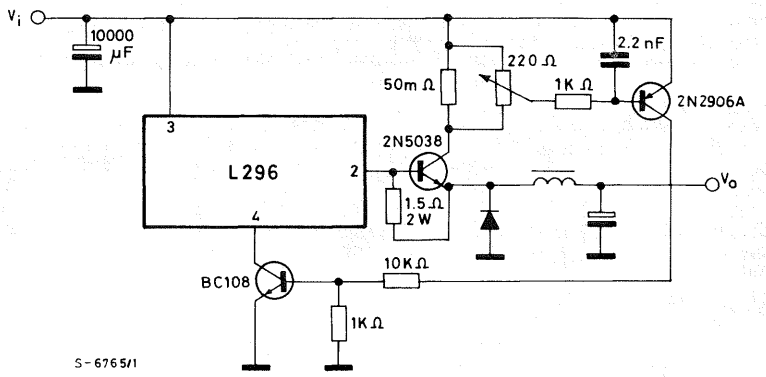
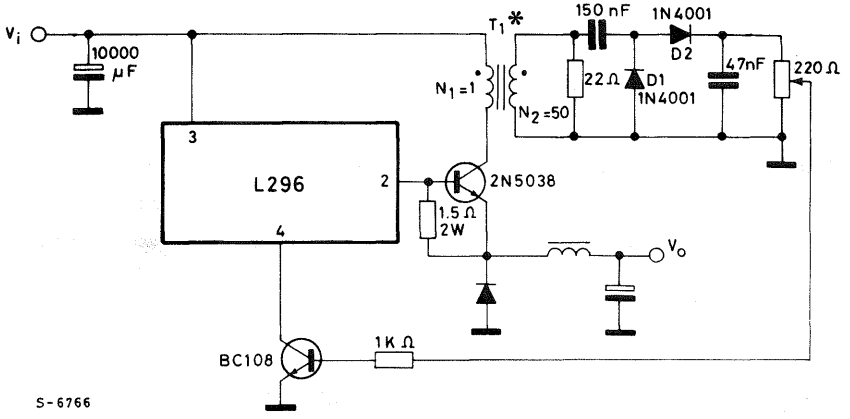


Fig. 39 – A small transformer is used in this example for current limiting.



* T_1 =MAGNETICS TOROID TYPE 55121-A2

STEP-UP CONVERTER

With the L296 it is also easy to realize a step-up converter, by using a MOS power transistor. Fig. 40 shows the electric diagram of the step-up converter. The frequency is 100 kHz, operation is in discontinuous mode and the device internal current limiter is used. Therefore no other external protection is required.

The input voltage could be a 12V car battery, from which an output voltage of 35V may be obtained. Lower output voltage values may be obtained by reducing the value of R_7.

DESCRIPTION OF OPERATION

Fig. 41 shows the diagram of the circuit realizing the step-up configuration.

When the transistor Q1 is ON, the inductance L charges itself with a current given by:

$$i_L = \frac{V_i}{L} t$$

The peak current in the coil is:

$$I_{peak} = \frac{V_i}{L} T_{ON}$$

Fig. 40 – A step-up converter using a power MOS transistor.

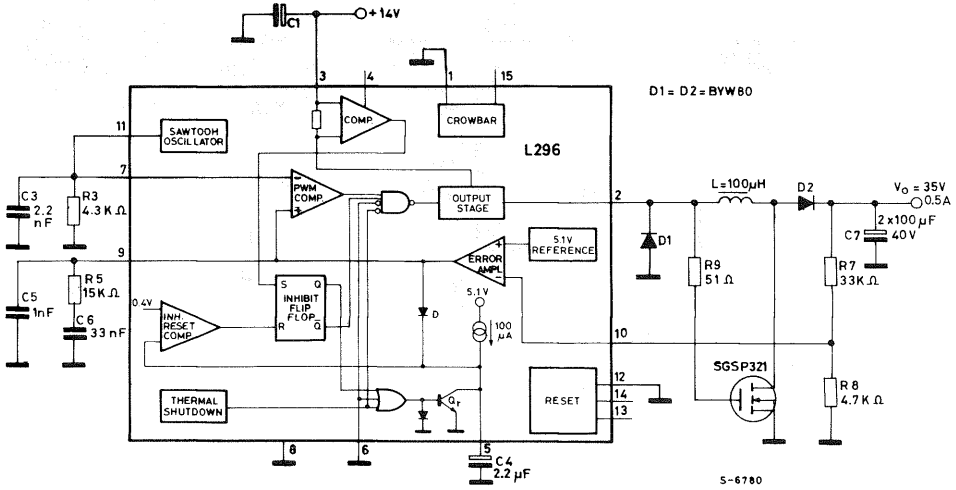
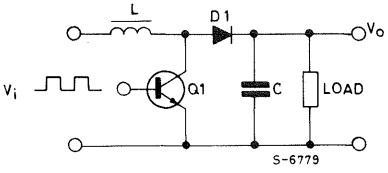


Fig. 41 – Basic schematic for step-up configurations.



In this configuration, unlike the step-down configuration, the peak current is not strictly related to the load current. The energy stored in the coil is successively discharged across the load when the transistor switches OFF. To calculate the I_o load current, the following procedure may be used:

$$\frac{1}{2} L I_{peak}^2 = V_o I_o T$$

$$I_o = \frac{L I_{peak}^2}{2 V_o T} = \frac{V_i^2 T_{ON}^2}{2 L V_o T}$$

For a greater output power to be available, the internal limitation must be replaced by an external circuit to protect the external power devices and to limit the current peak to a convenient value. A dual comparator (LM393) with hysteresis is used to avoid uncertainties when the current limitation operates. The electric diagram is shown in fig. 42.

LAYOUT CONSIDERATIONS

Both for linear and switching power supplies when the current exceeds 1A a careful layout becomes important to achieve a good regulation. The problem becomes more evident when designing switching regulators in which pulsed currents are over imposed on dc currents. In drawing the layout, therefore, special care has to be taken to separate ground paths for signal currents and ground paths for load currents, which generally show a much higher value.

When operating at high frequencies the path length becomes extremely important. The paths introduce distributed inductances, producing ringing phenomena and radiating noise into the surrounding space.

The recirculation diode must be connected close to pin 2, to avoid giving rise to dangerous extra negative voltages, due to the distributed inductance.

Fig. 43 and fig. 44 respectively show the electric diagram and the associated layout which has been realized taking these problems into account. Greater care must be taken to follow these rules when two or more mutually synchronized devices are used.

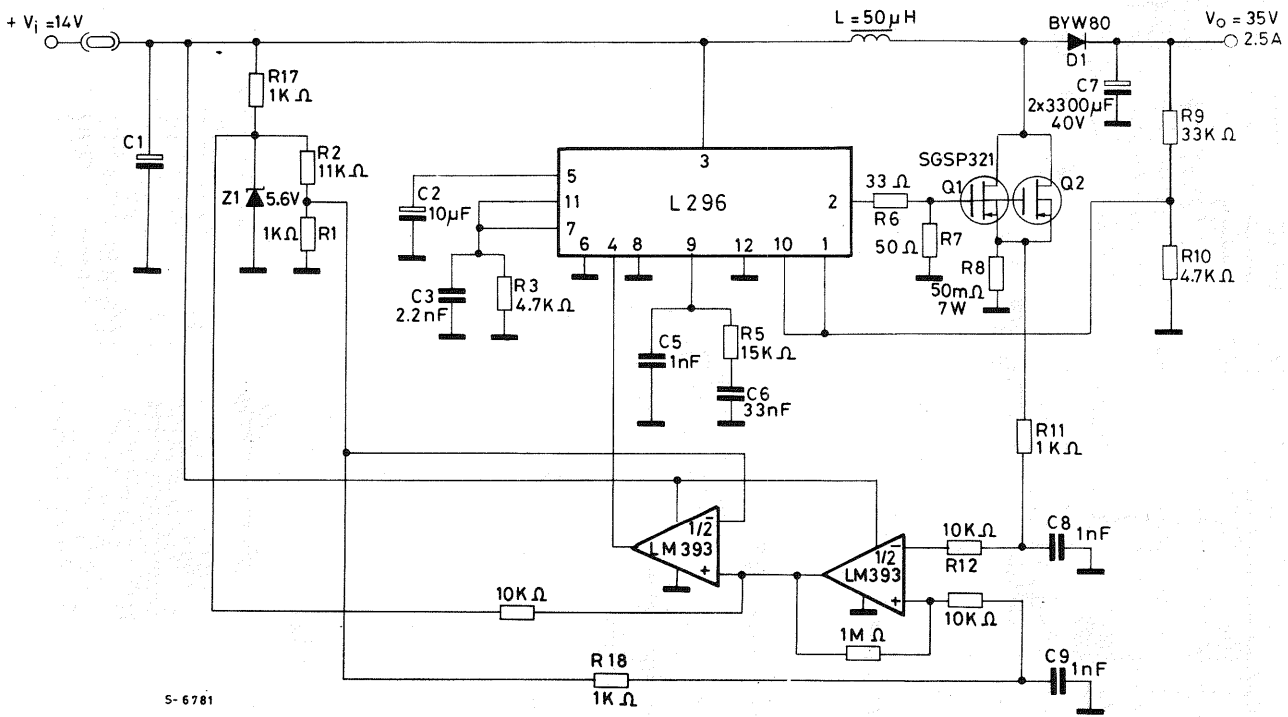
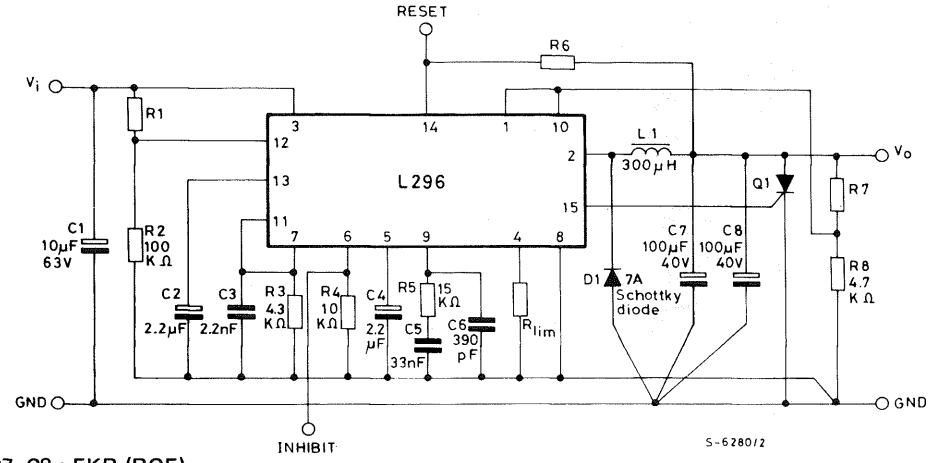


Fig. 42 – High power step-up converter showing how the current limiting function is realized externally.

Fig. 43 – Typical application circuit showing how the signal and power grounds are connected.



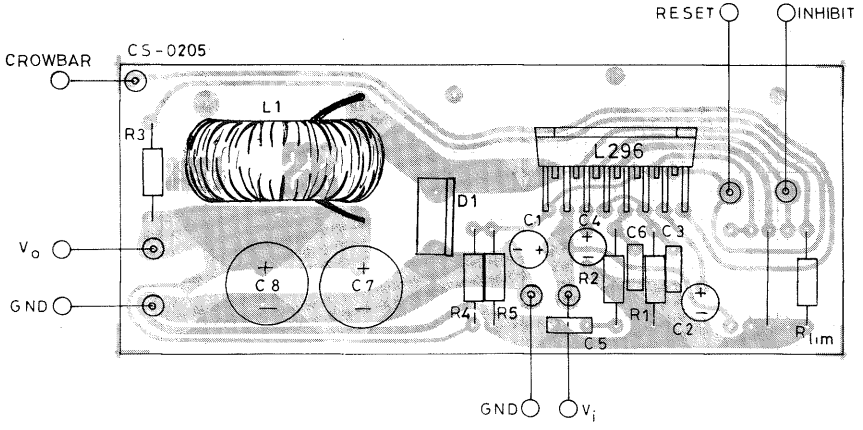
C7, C8 : EKR (ROE)

Suggested Inductor (L1)

Core Type	No Turns	Wire Gauge	Air Gap
Magnetics 58930 - A2MPP	43	1.0 mm.	–
Thomson GUP 20x16x7	65	0.8 mm.	1 mm.
Siemens EC 35/17/10 (B6633& - G0500 - X127)	40	2 x 0.8 mm.	–
VOGT 250 μH Toroidal coil, part number 5730501800			

Resistor values for standard output voltages		
V_o	R8	R7
12V	4.7 kΩ	6.2 kΩ
15V	4.7 kΩ	9.1 kΩ
18V	4.7 kΩ	12 kΩ
24V	4.7 kΩ	18 kΩ

Fig. 44 – A suitable PCB layout for the figure 43 circuit realized in accordance with the suggestions in the text (1 : 1 scale).



HEATSINK DIMENSIONING

The heatsink dissipates the heat produced by the device to prevent the internal temperature from reaching values which could be dangerous for device operation and reliability.

Integrated circuits in plastic package must never exceed 150 °C even in the worst conditions. This limit has been set because the encapsulating resin has problems of vitrification if subjected to temperatures of more than 150 °C for long periods or of more than 170°C for short periods. In any case the temperature accelerates the ageing process and therefore influences the device life; an increase of 10°C can halve the device life. A well designed heatsink should keep the junction temperature between 90°C and 110°C. Fig. 45 shows the structure of a power device. As demonstrated in thermodynamics, a thermal circuit can be considered to be an electrical circuit where R_1, R_2 represent the thermal resistance of the elements (expressed in °C/W) (see fig. 46).

Fig. 45

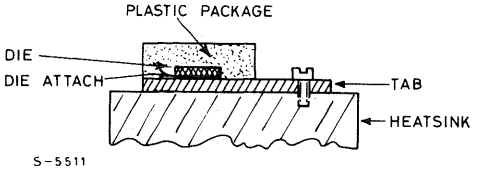
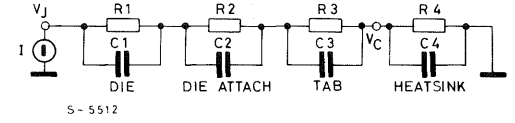


Fig. 46

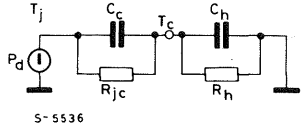


C1, C2 are the thermal capacitance (expressed in °C/W)
I is the dissipated power
V is the temperature difference with respect to the reference (ground)

This circuit can be simplified as shown in fig. 47, where:

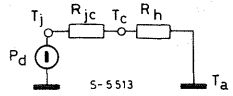
C_c is the thermal capacitance of the die plus that of the tab.
C_h is the thermal capacitance of the heatsink
R_{jc} is the junction case thermal resistance
R_h is the heatsink thermal resistance

Fig. 47



But since the aim of this section is not that of studing the transistors, the circuit can be further reduced as shown in figure 48.

Fig. 48



If we now consider the ground potential as ambient temperature, we have:

$$T_j = T_a + (R_{jc} + R_h) P_d \quad a)$$

$$R_h = \frac{T_j - T_a - R_{jc} P_d}{P_d} \quad b)$$

$$T_c = T_a + R_h P_d \quad c)$$

Thermal contact resistance depends on various factors such as the mounting, contact area and planarity of the heatsink. With no material between the device and heatsink the thermal resistance is around 0.5 °C/W; with silicone grease roughly 0.3 °C/W and with silicone grease plus a mica insulator about 0.4 °C/W. See fig. 49. In application where one external transistor is used together, the dissipated power must be calculated for each component. The various junction temperatures can be calculated by solving the circuit shown in fig. 50. This applies if the dissipating elements are fairly close with respect to the dissipator dimensions, otherwise the dissipator can no longer be considered as a concentrated constant and the calculation becomes difficult. This concept is better explained by the graph in fig. 51 which shows the case (and therefore junction) temperature variation as a function of the distance between two dissipating elements with the same type of heatsink and the same dissipated power. The graph in fig. 51 refers to the specific case of two elements dissipating the same power, fixed on a rectangular aluminium plate with a ratio of 3 between the two sides. The temperature jump will depend on the total dissipated power and on the devices geometrical positions. We want to show that there exists an optimal position between the two devices:

$$d = \frac{1}{2} \cdot \text{ side of the plate}$$

Fig. 49

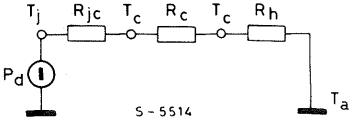


Fig. 50

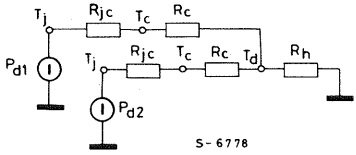


Fig. 52 shows the trend of the temperature as a function of the distance between two dissipating elements whose dissipated power is fairly different (ratio 1 to 4). This graph may be useful in application with two L296 synchronized.

Fig. 51

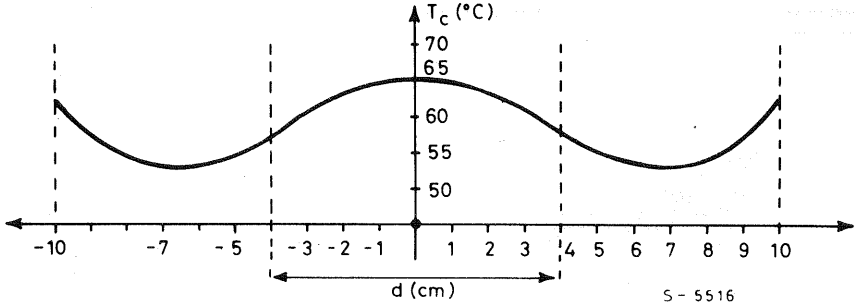
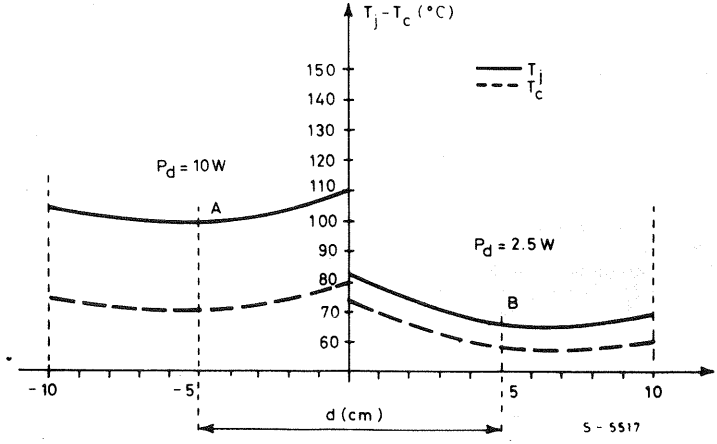


Fig. 52



APPENDIX A: CALCULATING SYSTEM STABILITY

This section is intended to help the designer in the calculation of the stability of the whole system.

Figure A1 shows the entire control system of the switching regulator.

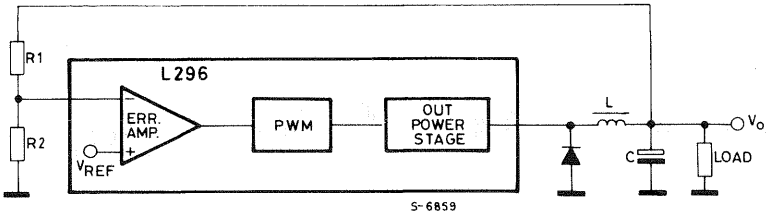
The problem which arises immediately is the transfer function of the PWM block and output stage, which is non-linear. If this function can be considered linear the analysis is greatly simplified.

Since the circuit operates at a constant frequency and the internal logic is fairly fast, the error introduced by assuming that this function is linear is minimized. Factors which could contribute to the non-linearity are an excessive delay in the output power transistor, ringing and parasitic oscillations generated in the power stage and non-linearity introduced by magnetic part.

In the case of the L296, in which the power transistor is internal and driven by well-controlled and efficient logic, the contribution to non-linearity is further reduced.

For the assumption of linearity to be valid the cut-off frequency of the LC filter must be much lower than the switching frequency. In fact, switching operation introduces singularities (poles) at roughly half the switching frequency. Consequently, as long as the LC filter is still dominant, its cut-off frequency must be at least an order of magnitude lower than the switching frequency. This condition is not, however, difficult to respect. The characteristics of LC filter affect the output voltage waveforms; is generally much less than an order of magnitude below the switching frequency.

Fig. A1 – The control loop of the switching regulator.



GAIN OF THE PWM BLOCK AND OUTPUT STAGE

The equation which links V_o to V_i is:

$$V_o = V_i \frac{T_{ON}}{T}$$

A variation ΔT_{ON} in the conduction time of the switching transistor causes a corresponding variation in the output voltage, ΔV_o, giving:

$$\frac{\Delta V_o}{\Delta T_{ON}} = \frac{V_i}{T}$$

Indicating with V_r the output voltage of the error amplifier, and with V_{ct} the amplitude of the ramp (the difference between the maximum and minimum values), T_{ON} is zero when V_r is at the minimum value and equal to T when V_r is at a maximum. Consequently:

$$\frac{\Delta T_{ON}}{\Delta V_r} = \frac{T}{V_{ct}}$$

The gain is given by:

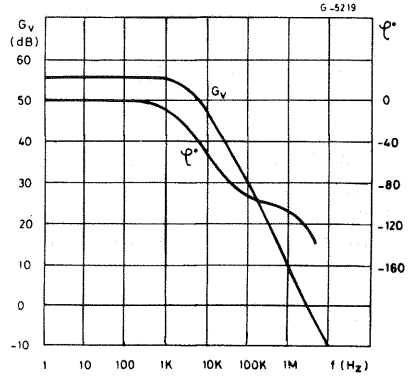
$$\frac{\Delta V_o}{\Delta V_r} = \frac{V_i}{V_{ct}}$$

Since V_{ct} is absolutely constant the gain of the PWM block is directly proportional to the supply voltage V_i.

ERROR AMPLIFIER

The error amplifier is a transconductance amplifier (it transforms a voltage variation at the input into a current variation at the output). It is used in open loop configuration inside the main control loop and its gain and frequency response are determined by a compensation network connected between its output and ground.

Fig. A2 – Open loop frequency and phase response of error amplifier.



In the application a series RC network is recommended which gives high system gain at low frequency – to ensure good precision and mains ripple rejection and a lower gain at high frequencies to ensure stability of the system. Figure A2 shows the gain and phase curves of the uncompensated error amplifier.

The amplifier has one pole at about 7 kHz and a phase shift which reaches about – 90° at frequencies around 1 MHz.

The introduction of a series network R_C C_C between the output and ground modifies the circuit as shown in figure A3.

Figure A4 shows the gain and phase curves of the compensated error amplifier.

Fig. A3 – Compensation network of the error amplifier.

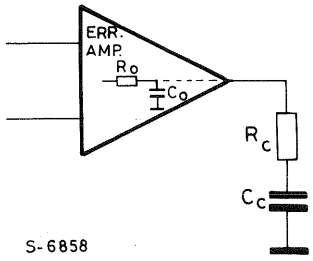
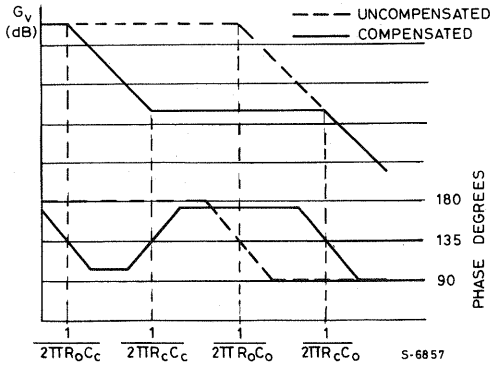


Fig. A4 – Bode plot showing gain and phase of compensated error amplifier.



CALCULATING THE STABILITY

For the stability calculation refer to the block diagram shown in figure A5.

The transfer functions of the various blocks are rewritten as follows.

The simplified transfer function of the compensated error amplifier is:

$$G_{EA} = g_m Z_c = g_m \frac{1 + s R_c C_c}{s C_c} \qquad (g_m = \frac{1}{2500})$$

The DC gain must be considered equal to

$$A_o = g_m R_o$$

PWM block and output stage:

$$G_{PWM} = \frac{V_i}{V_{ct}}$$

LC FILTER:

$$G_{LC} = \frac{1 + s\,C \cdot ESR}{s^2 LC + s\,C\,ESR + 1}$$

where ESR is the equivalent series resistance of the output capacitor which introduces a zero at high frequencies, indispensable for system stability. Such a filter introduces two poles at the angular frequency.

$$\omega_o = \frac{1}{\sqrt{LC}}$$

Refer to the literature for a more detailed analysis.

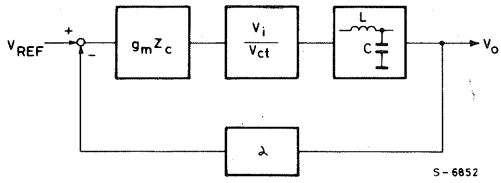
Feedback: consists of the block labelled α

$\alpha = 1$ when $V_o = V_{REF}$ (and therefore $V_o = 5.1V$)

and

$$\alpha = \frac{R_2}{R_1 + R_2} \quad \text{when } V_o > V_{REF}$$

Fig. A5 – Block diagram used in stability calculation



To analyse the stability we will use a Bode diagram. The values of L and C necessary to obtain the required regulator output performance, once the frequency is fixed, are calculated with the following formulae:

$$L = \frac{(V_i - V_o)\,V_o}{V_i\,f\,\Delta I_L}$$

$$C = \frac{(V_i - V_o)\,V_o}{8\,L\,f^2\,\Delta V_o}$$

Since this filter introduces two poles at the angular frequency

$$\omega_o = \frac{1}{\sqrt{LC}}$$

we place the zero of the R_c C_c network in the same place:

$$\omega_z = \frac{1}{R_c C_c}$$

Taking into account also the gain of the PWM block, the Bode plot of figure A6 is obtained.

The slope where the curve crosses the axis at 0 dB is about 40dB/decade therefore the circuit is unstable.

Taking into account now the zero introduced by the equivalent series resistance (ESR) of the output capacitor, we have further condition for dimensioning the R_c C_c network. Knowing the ESR (which is supplied by the manufacturer for the quality components) we can determine the value of R_c so that the axis is crossed at 0dB with a single slope. The zero introduced by the ESR is at the angular frequency:

$$\omega_{zESR} = \frac{1}{ESR \cdot C}$$

The overall Bode diagramm is therefore as shown in figure A7.

Fig. A6 – Bode plot of system taking filter and compensation network into account.

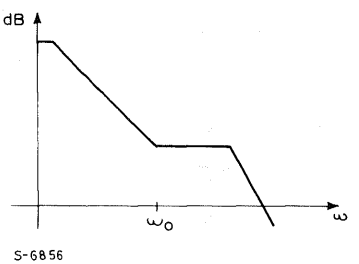
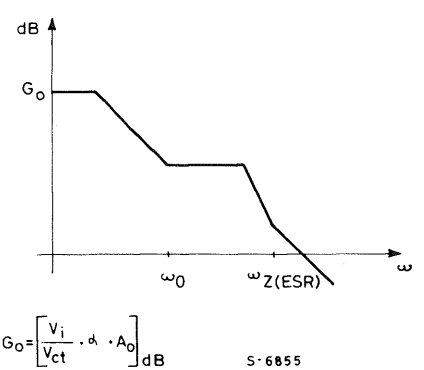


Fig. A7 – Bode plot of complete system taking into consideration the equivalent series resistance of the output capacitor.



DC GAIN AND LINE REGULATION

Indicating the open-loop gain of the error amplifier with A_o, the overall open-loop gain of the system is:

$$A_t = A_o \frac{V_i}{V_{ct}} \cdot \frac{R_2}{R_1 + R_2}$$

When $V_o = V_{REF}$, the gain becomes:

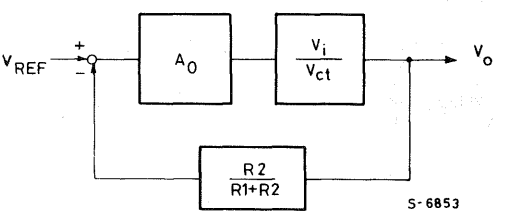
$$A_t = A_o \frac{V_i}{V_{ct}}$$

Considering the block diagram of figure A8 and calculating the output variation ΔV_o caused by a variation of V_i, from the literature we obtain:

$$\frac{\frac{\Delta V_o}{V_o}}{\frac{\Delta V_i}{V_i}} = \frac{1}{\frac{A_o V_i}{V_{ct}} \cdot \frac{R_2}{R_1 + R_2}}$$

This espression is of general validity. In our case the percentage variation of the reference must be added by vector addition.

Fig. A8 – Block diagram for calculation of line regulation.



APPENDIX B: REDUCING INTERFERENCE

The main disadvantage of the switching technique is the generation of interference which can reach levels which cause malfunctions and interfere with other equipment.

For each application it is therefore necessary to study specific means to reduce this interference within the limits allowed by the appropriate standards.

Among the main sources of noise are the parasitic inductances and capacitances within the system which are charged and discharged fastly. Parasitic capacitances originate mainly between the device case and the heatsink, the windings of the inductor and the connection wires. Parasitic inductances are

generally found distributed along the strips of the printed circuit board.

Fast switching of the power transistors tends to cause ringing and oscillations as a result of the parasitic elements. The use of a diode with a fast reverse recovery time (trr) contributes to a reduction in the noise flowing by the current peak generated when the diode is reverse biased.

Radiated interference is usually reduced by enclosing the regulator in a metal box.

To reduce conducted electromagnetic interference (or radio frequency interferences – RFI) to the levels permitted a suitably dimensioned filter is added on the supply line. The best method, generally, to reduce conducted noise is to filter each output terminal of the regulator. The use of a fixed switching frequency allows the use of a filter with a relatively narrow bandwidth. For off-line switching regulators this filter is usually costly and bulky. In contrast, if the device is supplied from a 50/60 Hz transformer the RFI filter problem is greatly reduced.

Tests have been carried out at the laboratories of Roederstein to determine the dimensions of a mains supply filter which satisfies the VDE 0871/6.78, class B standard. The measurements (see figs. B1 and B2) refer to the application with the L296 supplied with a filtered secondary voltage of about 30V, with V_o = 5.1V and I_o = 4A. The switching frequency is 100 kHz.

Figure B1 shows the results obtained by introducing on the transformer primary a 0.01 μF/250V~ class X capacitor (type ERO F1772-310-2030). To reduce interference further below the limit set by the standards an additional inductive filter must be added on the primary of the transformer.

Figure B2 shows the curves obtained by introducing this inductive filter (type ERO F1753-210-124).

Measurements have also been performed beyond 30 MHz; the maximum value measured is still well below the limit curve.

Fig. B1 – EMI measurements with a capacitor connected across the primary transformer with screen grounded (A) and floating (B)

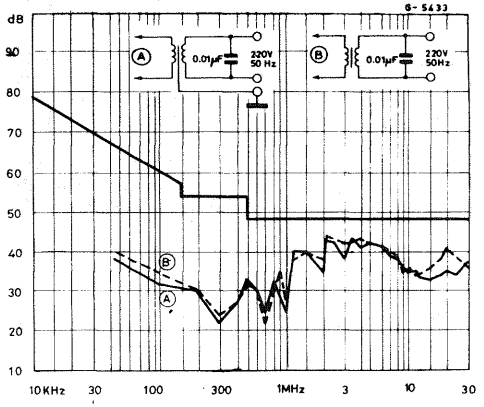
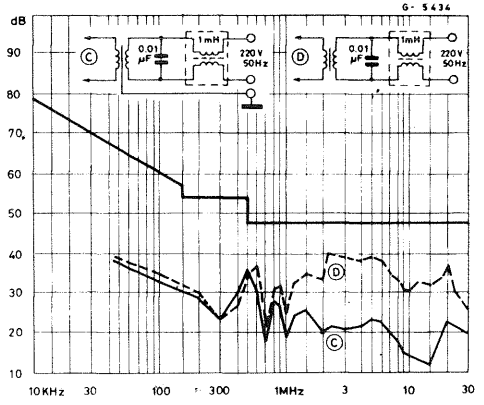


Fig. B2 – EMI results with the addition of an inductive filter on the mains input.



DESIGNING MULTIPLE-OUTPUT POWER SUPPLIES WITH THE L296 AND L4960

Multiple output supplies can be realized simply and economically using the SGS L296 and L4960 high power switching regulators. This note describes several practical circuits of this type.

Most of the switching regulators produced today have multiple outputs. The output voltages most frequently used – at least for powers up to 50W - are +5V -5V, +12V and -12V. In these supplies the 5V output is normally the output which delivers the highest current and requires the highest precision. For the other voltages – particularly the negative outputs – less precision (±5% ±7%) is usually sufficient. Often, however, for high current 12V outputs better stabilization and greater precision (typically ±4% - the output tolerance of an L7800 series linear regulator) are required.

Multiple output supplies which satisfy these requirements can be realized using the SGS L296 and L4960 high power switching regulator ICs, Several practical supply designs are described below to illustrate how these components are used to build compact and inexpensive multi-output supplies.

DUAL OUTPUT 15W SUPPLY

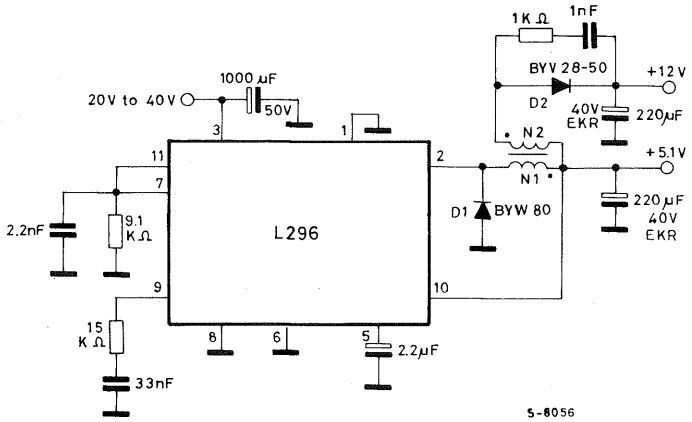
V_{o1} = 5V/3A, V_{o2} = 12V/150mA

A single L296 is used in this application to produce two outputs. The application circuit, Figure 1, illustrates how the second output (12V) is obtained by adding a second winding to the output inductor. Energy is transferred to the secondary during the recirculation period when the internal power device of the L296 is OFF.

Since the 12V output is not separated from the 5V output fewer turns are necessary for the second winding, therefore less copper is needed and load regulation is improved.

In applications of this type it is a good rule to ensure that the power drain on the auxiliary output is no more than 20-25% of the power delivered by the main output.

Fig. 1 - Dual output DC-DC converter (5V/3A, 12V/150mA)



Transformer: magnetics 58930, N1 = 30 turns, N2 = 40 turns

Table 1 shows the performance obtained with this dual output supply. This circuit operates at a switching frequency of 50KHz.

TABLE 1

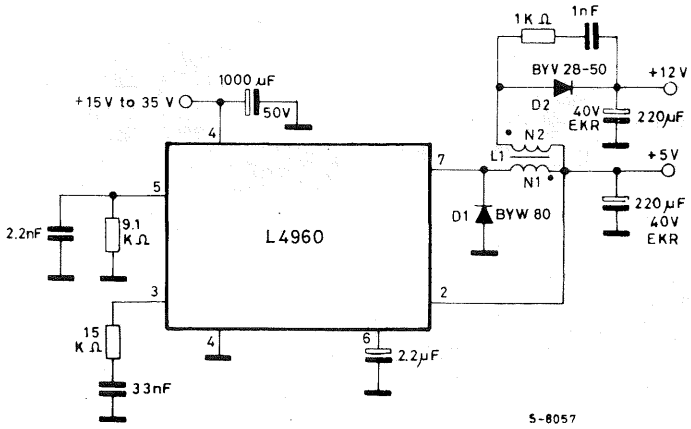
Parameter		V_{o1}	V_{o2}	Unit
Output voltage I_{o1} = 3A	V_i = 30V I_{o2} = 150mA	5.120	12.089	[V]
Output ripple		70	40	[mV]
Line regulation I_{o1} = 3A	20V ⩽ V_i ⩽ 40V I_{o2} = 150mA	15	30	[mV]
Line regulation I_{o1} = 700mA	20V ⩽ V_i ⩽ 40V I_{o2} = 100mA	15	10	[mV]
Load regulation I_{o1} = 700mA → 3A	V_i = 30V I_{o2} = 150mA	10	130	[mV]
Load regulation I_{o1} = 700mA	V_i = 30V I_{o2} = 100 → 150mA	0	40	[mV]
Load regulation I_{o1} = 3A	V_i = 30V I_{o2} = 100 → 150mA	0	40	[mV]
Efficiency	V_i = 30V V_{o1} = 5.120V I_{o1} = 3A V_{o2} = 12.089V I_{o2} = 150mA	75		%

DUAL OUTPUT 7.5W SUPPLY

V_{o1} = 5V/1.5A, V_{o2} = 12V/100mA

The same technique - adding a secondary winding - can also be used to produce an economical and simple dual output supply with the L4960, a device containing the same control loop blocks as the L296 and a 2A output stage. (Fig. 2). Though this circuit costs very little the performance obtained (see Table 2) is more than satisfactory. The switching frequency is 50kHz.

Fig. 2 - Dual output DC-DC converter (5V/1.5A, 12V/100mA)



Transformer: magnetics 58206, N1 = 30 turns, N2 = 40 turns

TABLE 2

Parameter		V_{o1}	V_{o2}	Unit
Output voltage I_{o1} = 1.5A	V_i = 25V I_{o2} = 100mA	5.050	12.010	[V]
Output ripple		50	30	[mV]
Line regulation I_{o1} = 1.5A	15V ⩽ V_i ⩽ 35V I_{o2} = 100mA	7	75	[mV]
Line regulation I_{o1} = 500mA	15V ⩽ V_i ⩽ 35V I_{o2} = 50mA	7	60	[mV]
Load regulation I_{o1} = 0.5A → 1.5A	V_i = 25V I_{o2} = 100mA	3	100	[mV]
Load regulation I_{o1} = 500mA	V_i = 25V I_{o2} = 50mA → 100mA	0	55	[mV]
Load regulation I_{o1} = 1.5A	V_i = 25V I_{o2} = 50mA → 100mA	0	50	[mV]
Efficiency	V_i = 25V I_{o1} = 1.5A I_{o2} = 100mA	78		%

TRIPLE OUTPUT 15W SUPPLY

V_{o1} = 5V/3A, V_{o2} = 12V/100mA, V_{o3} = -12V/100mA

Figure 3 shows how to obtain two auxiliary outputs (± 12V) which are isolated from the 5V output. For this output power range an L296 is used.

To ensure good tracking of the 12V and -12V outputs the secondary outputs in this application should be bifilar wound.

This circuit operates at 50KHz and gives the performance indicated in Table 3.

Fig. 3 - Triple output DC-DC converter (5V/3A, 12V/100mA, -12V/100mA)

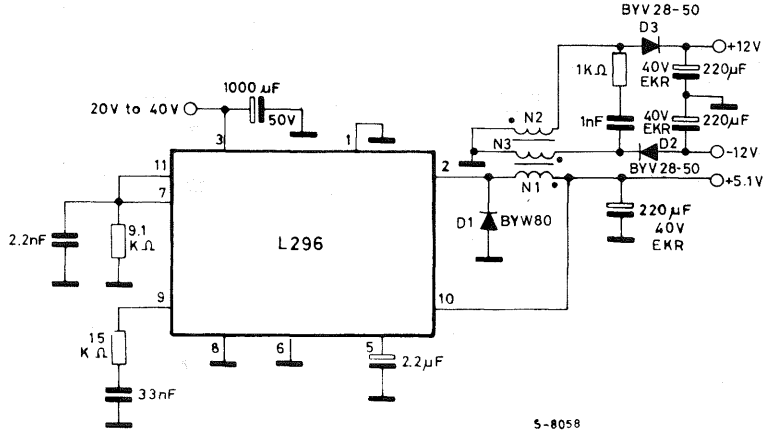


TABLE 3

Parameter		V_{o1}	V_{o2}	V_{o3}	Unit
Output Voltage I_{o1} = 3A	V_i = 30V $I_{o2} = I_{o3}$ = 100mA	5.057	12.300	-12.300	[V]
Output ripple		80	30	30	[mV]
Line regulation I_{o1} = 700mA	$20 \leqslant V_i \leqslant 40V$ $I_{o2} = I_{o3}$ = 100mA	15	60	60	[mV]
Line regulation I_{o1} = 3A	$20 \leqslant V_i \leqslant 40V$ $I_{o2} = I_{o3}$ = 100mA	18	100	100	[mV]
Load regulation I_{o1} = 0.7 → 3A	V_i = 30V $I_{o2} = I_{o3}$ = 100mA	4	150	150	[mV]
Load regulation I_{o1} = 3A	V_i = 30V I_{o2} = 100mA I_{o3} = 50 → 100mA	0	125	52	[mV]
Load regulation I_{o1} = 3A I_{o2} = 50 → 100mA	V_i = 30V I_{o3} = 100mA	0	50	120	[mV]
Efficiency		76			%

TRIPLE OUTPUT 7.5W SUPPLY

V_{o1}= 5V/1.5A, V_{o2}= 12V/50mA, V_{o3}= -12/50mA

For lower output powers, the L296 in the previous application may be replaced by an L4960 as shown in Figure 4. The performance of this circuit is indicated in Table 4.

Fig. 4 - Triple output DC-DC converter (5V/1.5A, 12V/50mA, -12V/50mA)

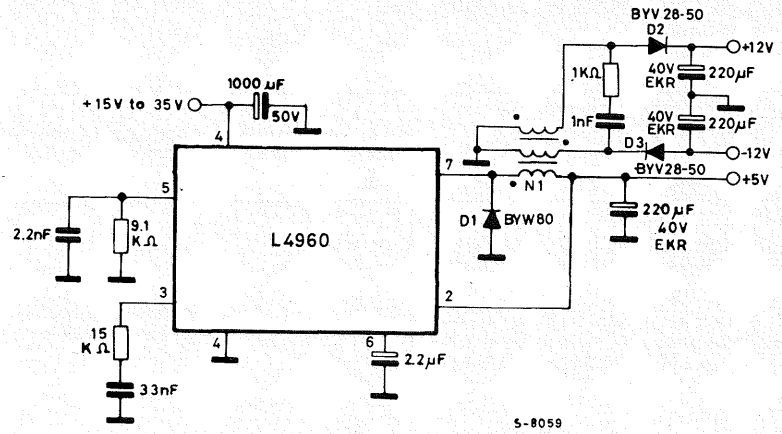


TABLE 4

Parameter		V_{o1}	V_{o2}	V_{o3}	Unit
Output Voltage I_{o1} = 1.5A	V_i = 25V $I_{o2} = I_{o3}$ = 50mA	5.040	12.020	-12.020	[V]
Output ripple		60	30	30	[mV]
Line regulation I_{o1} = 500mA	$15 \leqslant V_i \leqslant 35V$ $I_{o2} = I_{o3}$ = 50mA	5	80	80	[mV]
Line regulation I_{o1} = 1.5A	$15 \leqslant V_i \leqslant 35V$ $I_{o2} = I_{o3}$ = 50mA	4	60	60	[mV]
Load regulation I_{o1} = 0.5 → 1.5A	V_i = 25V $I_{o2} = I_{o3}$ = 50mA	5	120	120	[mV]
Load regulation I_o = 1.5A I_{o3} = 20 → 50mA	V_i = 25V I_{o2} = 50mA	0	15	50	[mV]
Load regulation I_{o1} = 1.5A I_{o2} = 20 → 50mA	V_i = 25V I_{o3} = 100mA	0	50	15	[mV]
Efficiency			70		%

THE L296 AND L4960 HIGH POWER SWITCHING REGULATORS

The SGS L296 is a monolithic stepdown switching regulator assembled in the 15-pin Multiwatt package. Operating with supply input voltages up to 46V it provides a regulated 4A output variable from 5.1V to 40V.

Internally the device is equipped with current limiter, soft start and reset (or power fail) functions, making it particularly suitable for supplying microprocessors and logic.

The precision of the L296's internal reference (±2%) eliminates the need for external dividers or trimming to obtain a 5V output.

The synchronization pin allows synchronous operation of several devices at the same frequency to avoid generating undesirable beat frequencies.

The L4960 is a similar device assembled in the 7-lead Heptawatt package. Like the L296 it has a maximum input voltage of 46V and it provides a regulated output voltage variable from 5V to 40V with a maximum load current of 2.5A. Current limiting, soft start and thermal protection functions are included.

The thermal protection circuit in both the L296 and L4960 has a hysteresis of 30°C to allow soft restarting after a fault condition.

THE STEP DOWN CONFIGURATION

Figure 5 shows the basic structure of a step down switching regulator. The transistor Q is used as a switch and the ON and OFF times are determined by the control circuit.

When Q is saturated current flows from the supply, Vi, to the load through the inductor L. Neglecting the saturation voltage of Q, Ve ≃ Vi.

When Q is OFF, current continues to flow in the inductor L, in the same direction, forcing the diode into conduction immediately therefore Ve is negative. In these conditions the load current flows through L and D.

The average value of the current in the inductor is equal to the load current. In the inductor a triangular current ripple equal to ΔI_L is added to this average current.

During the time when Q is ON this ripple is :

$$\Delta I_L = \frac{(V_i - V_o)\ T_{ON}}{L}$$

and when Q is off it is:

$$\Delta I_L = \frac{V_o \cdot T_{OFF}}{L}$$

Equating these expression and assuming that the transistor and diode are ideal we obtain :

$$V_o = V_i \cdot \frac{T_{ON}}{T}$$

T_{ON} is the conduction time of the transistor

T is the oscillator period

The absolute average current in the sypply is therefore :

$$I_{ioc} = I_o \cdot \frac{T_{ON}}{T}$$

Once the working frequency and desired ripple current have been fixed the value of the inductor L is given by :

$$L = \frac{(V_i - V_o)\ V_o}{V_i\ f\ \Delta I_L}$$

and the value of the capacitor C required to give the desired output voltage ripple (ΔV) is :

$$C = \frac{(V_i - V_o)\ V_o}{8\ L f^2\ \Delta f_o}$$

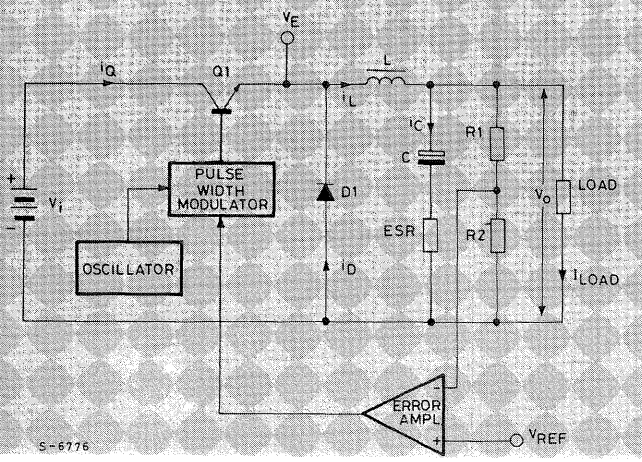
This capacitor must have a maximum ESR given by :

$$ESR_{MAX} = \frac{\Delta V_o}{\Delta I_L}$$

And, finally, the minimum load current, I_{OMIN}, must be :

$$I_{OMIN} = \frac{\Delta I_L}{2} = \frac{(V_i - V_o)\ V_o}{2 V_i\ f_L}$$

Fig. 5 - Basic STEP-DOWN configuration



30W DC-DC CONVERTER

Designing power supplies in the 30-40W range is becoming increasingly difficult because it is here that there is the greatest need to maintain performance levels and reduce costs. The application proposed here is very competitive because it exploits new ICs to reduce size, number of components and assembly costs.

This solution, the DC-DC converter, compares very favourable with off-line switching supplies in terms of cost. DC-DC converters can, in fact, be realized even by designers with little experience and allows the convenience of working with low voltages, Off-line switching supplies are only preferable when the weight and size of the mains transformer in a DC-DC converter would be excessive.

In this circuit, figure 6 two devices are used, an L296 and an L4960. The L296 is used to supply a 5V output with a current of 3A and the auxiliary -5V/100mA output and the L4960 is used to provide the 12V/1.5A output and the auxiliary -12V/100mA output.

Fig. 6 - Multioutput DC-DC converter with L296 and L4960 (5V/3A, 12V/1.5A, -12V/100mA, -5V/100mA)

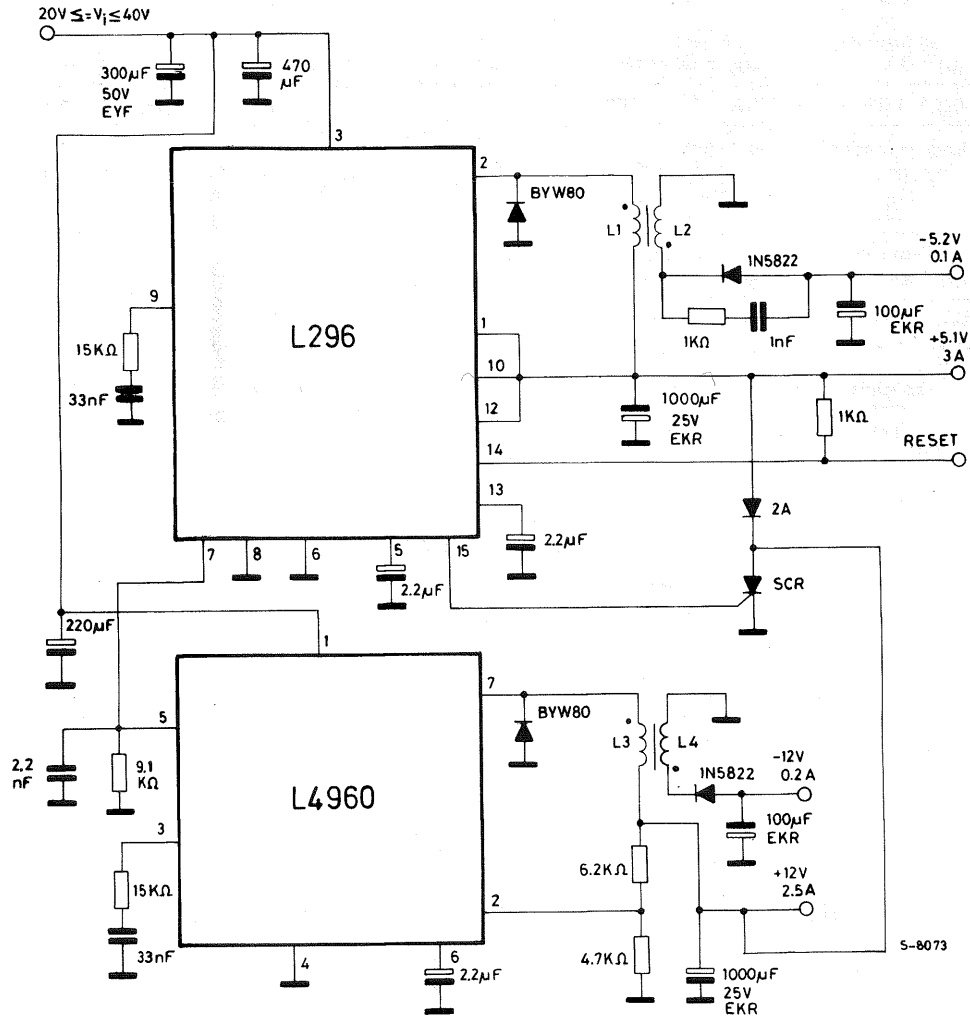


Table 5 shows the performance obtained with this power supply.

TABLE 5

Parameter		V_{o1}	V_{o2}	V_{o3}	V_{o4}	Unit
Output Voltage I_{o1} = 3A I_{o2} = 100mA	V_i = 30V I_{o3} = 1.5A I_{o4} = 100mA	5.080	-5010	11.96	12.00	[V]
Output ripple		50	30	50	40	[mV]
Line regulation I_{o1} = 1A I_{o3} = 0.5A	$20 \leqslant V_i \leqslant 40V$ I_{o2} = 100mA I_{o4} = 100mA	13	15	10	20	[mV]
Load regulation I_{o1} = 1A to 3A	V_i = 30V I_{o2} = 100mA	8	90			[mV]
I_{o3} = 0.5 to 1.5A	I_{o4} = 100mA			3	80	[mV]
Load regulation I_{o1} = 3A	V_i = 30V I_{o2} = 50 → 100mA	0	100			[mV]
I_{o3} = 1.5A	I_{o4} = 50 → 100mA			0	100	[mV]
Load regulation I_{o1} = 1A	V_i = 30V I_{o2} = 50 → 100mA	0	35			[mV]
I_{o3} = 0.5A	I_{o4}= 50 → 100mA			0	90	[mV]
Line regulation I_{o1} = 3A	$20 \leqslant V_i \leqslant 40V$ I_{o2} = 100mA	15	45			[mV]
I_{o3} = 1.5A	I_{o4} = 100mA			15	40	[mV]

This application illustrates how two devices may be synchronized. Note also that the reset circuit is used in this case to monitor the output voltage (see figure 7).

If a power fail function is required in place of the reset function the Figure 6 circuit should be modified as shown in Figure 8.

Fig. 7 - Reset output waveforms

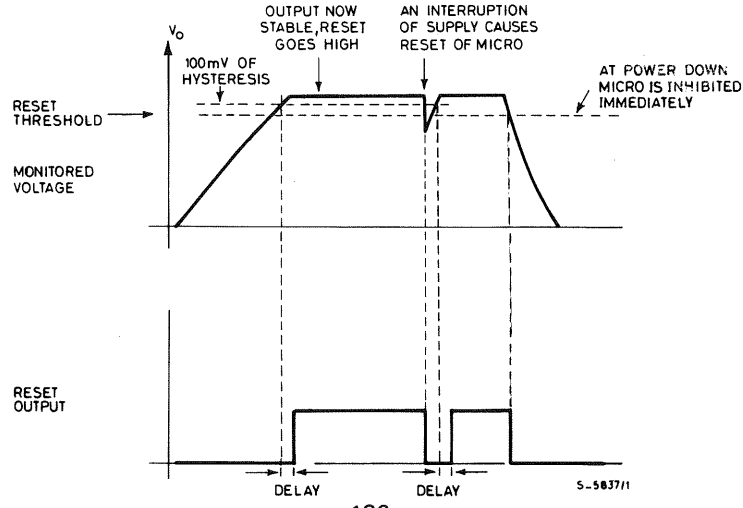
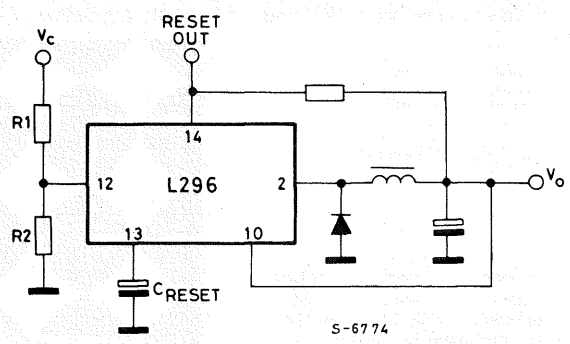


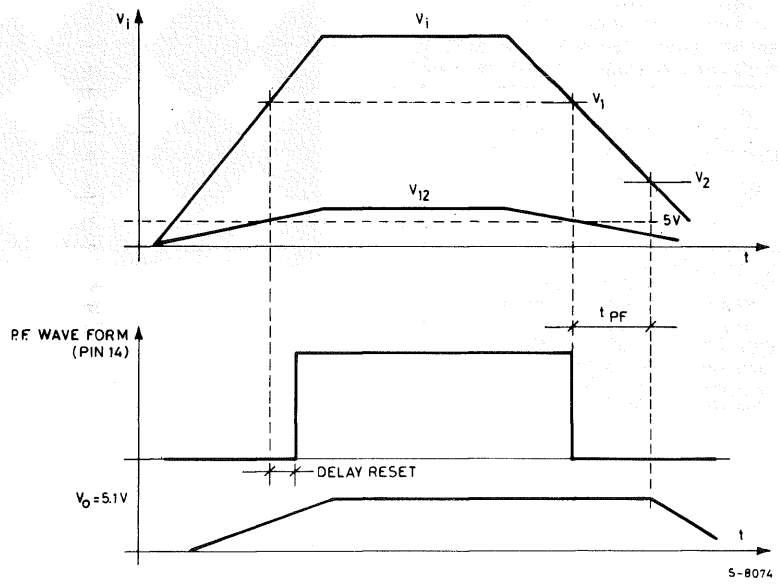
Fig. 8



CALCULATING THE POWER FAIL TIME

The 'power fail time' is defined as the time from when the power fail output (pin 14) goes low to the time when the input voltage falls to the minimum level required to maintain the regulated output (see Figure 9). From this definition we can evaluate the energy balance.

Fig. 9



The energy which the filter capacitor C supplies to the operating device while it discharges is:

$$E = 1/2C\,(V_1^2 - V_2^2) \qquad (1)$$

The load drains a power of $P_o = V_o\, I_o$. Taking into consideration the average efficiency η (derived with the input between V_1 and V_2), the power to be supplied at the input of the device is:

$$P_{o2} = \frac{P_o}{\eta} \qquad (2)$$

Equating the expressions (1) and (2) gives:

$$1/2C\,(V_1^2 - V_2^2) = \frac{P_o}{\eta} \cdot t_{PF}$$

where V_i is the input voltage at which the voltage on pin 12 reaches 5V (through the divider R_1/R_2); V_2 is the maximum input voltage below which the device no longer regulates.

Rearranging this expression to obtain C:

$$C = \frac{2\,P_o\,t_{PF}}{\eta\,(V_1^2 - V_2^2)}$$

EXAMPLE - Suppose that V_o = 5V, I_o = 3A, T_{pf} = 10ms and V_i = 35V. Fixing V_1 = 25V and V_2 = 10V we obtain:

$$C = \frac{2\,P_o\,t_{PF}}{\eta\,(V_1^2 - V_2^2)} = \frac{2 \times 15 \times 10 \cdot 10^{-3}}{0.75\,(25^2 - 10^2)} = 760\mu F$$

We therefore choose a capacitor of 1000μF.

CROWBAR

The L296 includes an internal crowbar function; the only external component needed is an SCR. The intervention threshold of this block is fixed internally at ± 20% of the nominal value of the internal reference.

In the Figure 6 circuit the SCR is triggered by an overvoltage on the 5V output (usually the most important output to monitor) and shortcircuits to ground the 5V output and, through the diode which connects the two outputs, the 12V output.

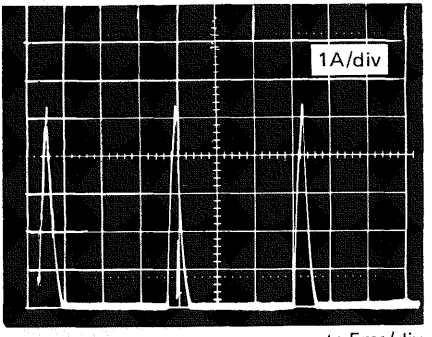
Since the internal current limiter in the device is designed to function as shown in Figure 10 (that is, with pulsed output current) the SCR turns off in the gap between pulses and is re-activated gain if, when the device restarts softly, the fault condition has not been eliminated. But if the fault no longer exists the SCR remains OFF and the output voltage returns to the normal value.

If the designer prefers the supply to remain off after the SCR has been activated the circuit can be modified as shown in Figure 11. In this modification, when the SCR is triggered a very high current flows in the fuse, blowing it.

Since the filter capacitor can have a high value and be charged to high voltages the choice of SCR is important. The type used in this circuit - the TYP512 - is a plastic packaged SCR able to handle 12Arms and 300A for 10ms. The maximum forward and reverse voltages are about 50V.

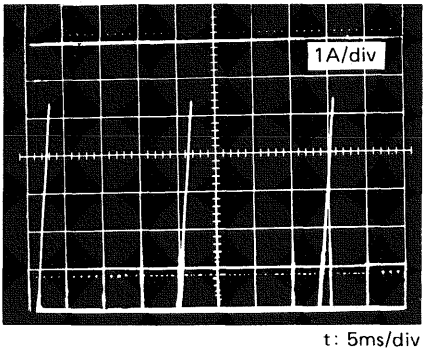
If the crowbar circuit is not used it is advisable to connect pin 1 to ground or pin 10.

Figs 10 - Load current in short circuit conditions (V_i = 40V, L = 300μH, f = 100KHz)



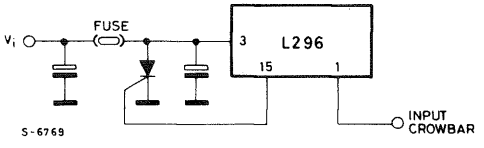
t: 5ms/div

Current at pin 2 when the output is short circuited.



t: 5ms/div

Fig. 11



POWER SUPPLY DESIGN BASICS

Aimed at system designers whose interest focusses on other fields, this note reviews the basic power supply design knowhow assumed in the rest of the book.

In mains-supplied electronic systems the AC input voltage must be converted into a DC voltage with the right value and degree of stabilization.

Figures 1 and 2 show the simplest rectifier circuits. In these basic configurations the peak voltage across the load is equal to the peak value of the AC voltage supplied by the transformer's secondary winding. For most applications the output ripple produced by these circuits is too high. However, for some applications - driving small motors or lamps, for example - they are satisfactory.

If a filter capacitor is added after the rectifier diodes the output voltage waveform is improved considerably. Figures 3 and 4 show two classic circuits commonly used to obtain continuous voltages starting from an alternating voltage. The Figure 3 circuit uses a center-tapped transformer with two rectifier diodes while the Figure 4 circuit uses a simple transformer and four rectifier diodes.

Fig. 1 - Basic half wave rectifier circuit

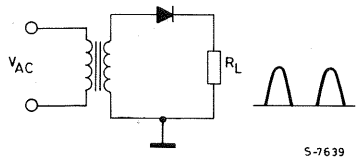


Fig. 2 - Full wave rectifier wich uses a center-tapped transformer

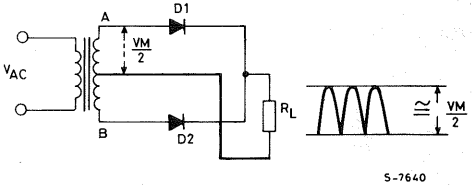


Fig. 3 - Full wave rectified output from the transformer/rectifier combination is filtered by C1

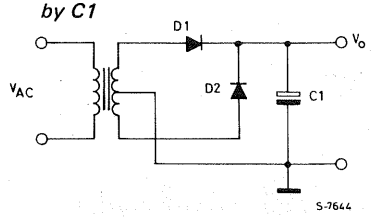


Fig. 4 - This circuit performs identically to that shown in Fig. 3

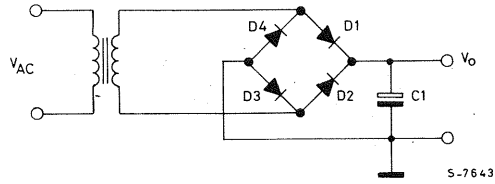


Figure 5 shows the continuous voltage curve obtained by adding a filter capacitor to the Figure 1 circuit. The section b-c is a straight line. During this time it is the filter capacitor that supplies the load current. The slope of this line increases as the current increases, bringing point c lower. Consequently the diode conduction time (c-d) increases, increasing ripple. With zero load current the DC output voltage is equal to the peak value of the rectified AC voltage.

Fig. 5 - Output waveforms from the half-wave rectifier filter

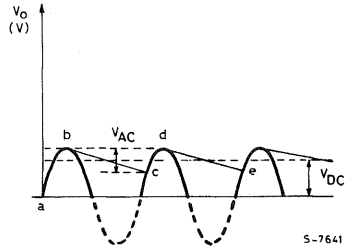


Figure 6 shows how to obtain positive and negative outputs referred to a common ground. Useful design data for this circuit is given in Figures 7, 8 and 9. In particular, the curves shown in Figure 7 are helpful in determining the voltage ripple for a given load current and filter capacitor value. The value of the voltage ripple obtained is directly proportional to the load current and inversely proportional to the filter capacitor value.

Fig. 6 - Full-wave split supply rectifier

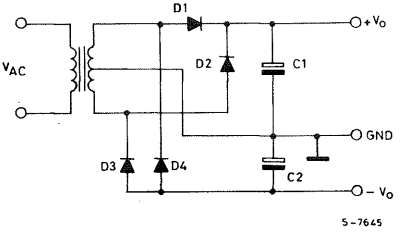


Fig. 7 - Ripple voltage vs. filter capacitor value (full-wave rectifier)

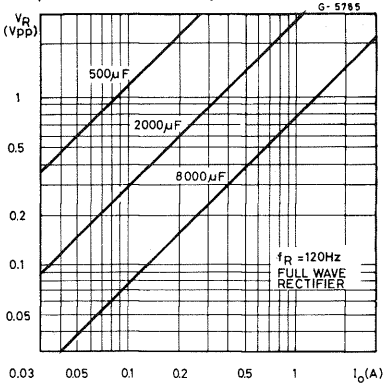


Fig. 8 - DC to peak ratio for half wave rectifiers

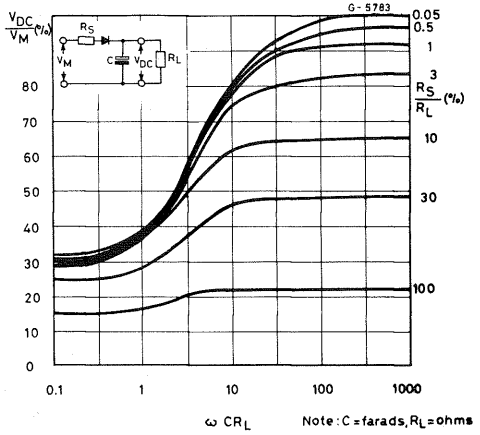
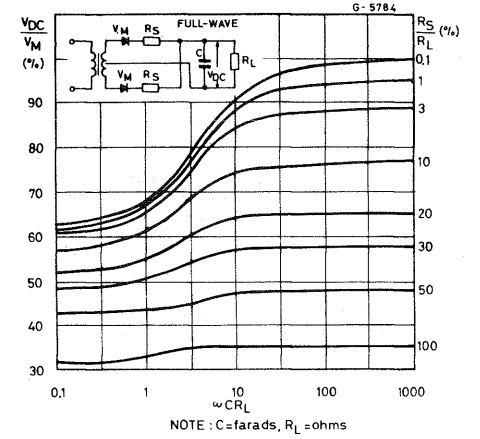


Fig. 9 - DC to peak ratio for full-wave rectifiers



The performance of a supply commonly used in consumer applications - in audio amplifiers, for example - is described in Figure 10 and Table 1.

Fig. 10 - DC characteristics of a 50VA non-regulated supply

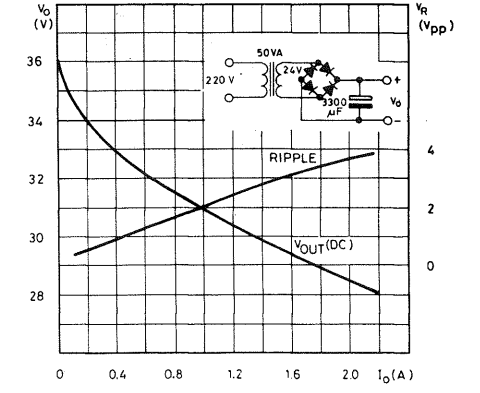


Table 1

Mains (220V)	Secondary voltage	DC output voltage (V_O)		
		$I_O = 0$	$I_O = 0.1A$	$I_O = 1A$
+20%	28.8V	43.2V	42V	37.5V
+15%	27.6V	41.4V	40.3V	35.8V
+10%	26.4V	39.6V	38.5V	34.2V
—	24V	36.2V	35V	31V
-10%	21.6V	32.4V	31.5V	27.8V
-15%	20.4V	30.6V	29.8V	26V
-20%	19.2V	28.8V	28V	24.3V

When a low ripple voltage is required an LC filter network may be used. The effect on the output voltage of this addition is shown in Figure 11. As Figure 11 shows, the residual ripple can be reduced by 40dB. But often the inductor is costly and bulky.

Often the degree of stability provided by the circuits described above is insufficient and a stabilizer circuit is needed. Figure 12 shows the simplest solution and is satisfactory for loads of up to about 50mA. This circuit is often used as a reference voltage to apply to the base of a transistor of to the input of an op amp to obtain higher output current.

The simplest example of a series regulator is shown in Figure 13. In this circuit the transistor is connected as a voltage follower and the output voltage is about 600-700mV lower than the zener voltage. The resistor R must be dimensioned so that the zener is correctly biased and that sufficient base current is supplied to the base of Q1.

For high load currents the base current of Q1 is no longer negligible. To avoid that the current in the zener drops to the point where effective regulation is not possible a darlington may be used in place of the transistor.

When better performance is required the op amp circuit shown in Figure 14 is recommended. In this circuit the output voltage is equal to the reference voltage applied to the input of the op amp. With a suitable output buffer higher currents can be obtained.

Fig. 11 - Ripple reduction produced by a single section inductance-capacitance filter

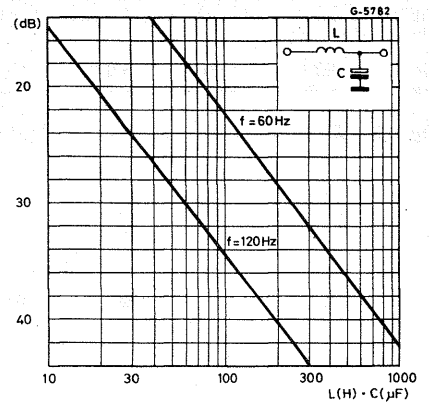


Fig. 12 - Basic zener regulator curcuit.

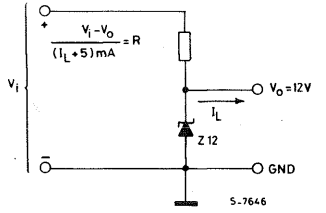


Fig. 13 - The series pass zener-based regulator circuit can supply load currents up to about 100mA

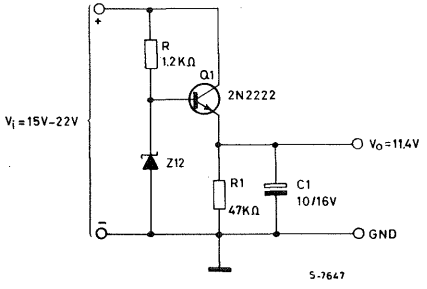
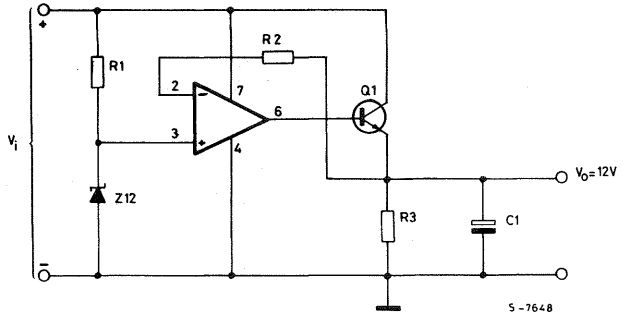


Fig. 14 - The Op-Amp-based regulator can supply 100mA with excellent regulation



The output voltage of the Figure 14 circuit can be varied by adding a variable divider in parallel with the zener diode and with its wiper connected to the op amp's input.

The design of stabilized supplius has been simplified dramatically by the introduction of voltage regulator ICs such as the L78xx and L79xx - three-terminal series regulators which provide a very stable output and include current limiter and thermal protection functions. Figures 16, 17 and 18 show how these circuits are used. Refer to the datasheets for more information.

Fig. 15 - Zener regulator circuit modified for low-noise output

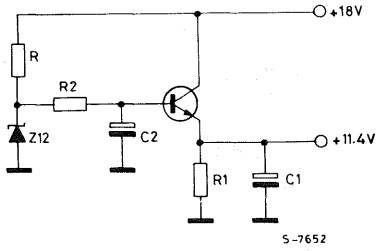


Fig. 16 - A three terminal 1A positive regulator circuit is very simple and performs very well.

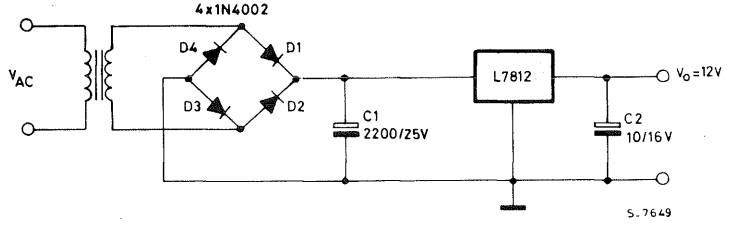


Fig. 17 - A three terminal 1A negative voltage regulator

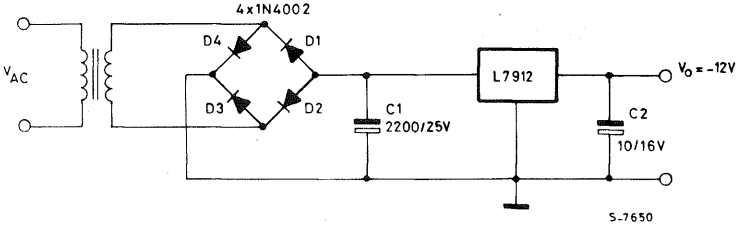
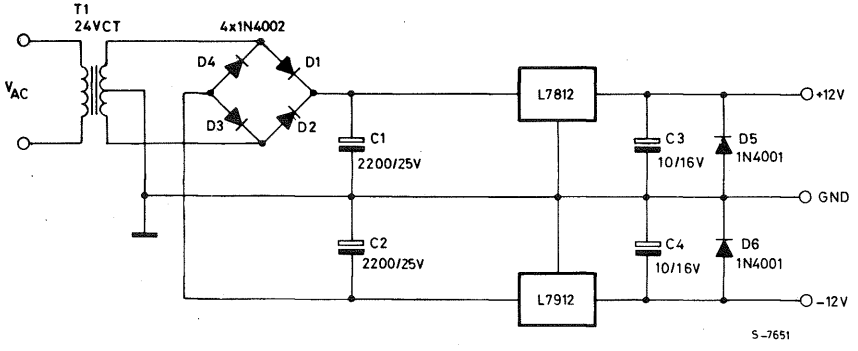


Fig. 18 - Complete ± 12V - 1A split supply regulator circuit



SUPPLY DESIGN FOR CMOS SRAMs AND SHADOW-TYPE NVRAMs

The L4901 and L4902 dual 5V regulators and the TL7700 supply controller simplify the design of systems using battery backup and non-volatile RAM. This note illustrates several typical application configurations.

The convenience of preserving data when equipment is turned off - deliberately or accidentally - has prompted may system designers to adopt low-power CMOS static RAMs with battery backup or shadow-type non-volative RAMs. Integrated circuits such as the TL077 power supply controller and the L4901/L4902 dual voltage regulators simplify the use of these memories and ensure dependable operation.

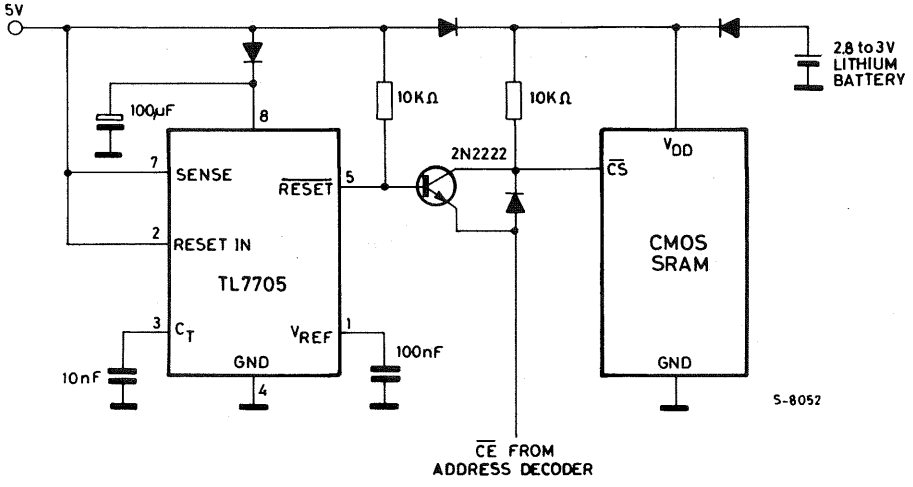
LOW POWER CMOS RAMs

CMOS static RAMs with a standby or low-power operating mode require a backup battery delivering 1μA at 2-3V to maintain memory contents in the stabdby state. Lithium cells are generally used as the backup supply but since these cells have a high internal resistance it is advisable to disable the RAM before selecting standby mode. Otherwise the drain on the battery will cause the voltage to fall so low that memory contents are corrupted.

Another design rule to remember is that the inputs of CMOS devices should never go more than 0.6V above the supply voltage or they could latch up.

These conditions can be satisfied by using a TL7705 supply controller with a conventional 5V supply, as shown in figure 1. In this circuit the TL7705's RESET output ensures that the CMOS RAM is not enabled when the main 5V supply is falling.

Fig. 1 - A TL7705 power supply controller can be used to ensure thata CMOS RAM isn't enabled when the 5V supply is removed



Another solution is to use an L4901 or L4902 dual 5V voltage regulator IC. These devices provide a reset output and two regulated voltage outputs. The first (V1) delivers up to 300mA and features a low leakage at the output when the input is not powered (less than 2μA); this output typically supplies standby circuits. The second output (V2) delivers up to 400mA and normally powers other 5V circuits which are powered down in the standby state. V1 is always higher than V2.

The difference between the two devices is that the L4901 (Fig. 4) has separate inputs for the V1 and V2 regulators while the L4901 has a common input and a disable input which deactivates the V2 output.

As shown in figure 2, the L4901 may be used with the V1 output supplying CMOS battery backup RAM and the V2 output supplying a microprocessor and other 5V chips. In this case the L4901's RESET output is used both to reset the Z80 and, through the M74HC138 address decoder, to ensure that the RAMs are disabled when the main supply is removed. Note that the M74HC138 is supplied from the backup battery. Devices of this high speed CMOS family accept a supply voltage from 2 to 6V and in static operation draw less than 4μA current. They are also very fast (t_{PD} = 17μs @ 5V), ideal for this kind of memory.

Fig. 2 - The dual output L4901 regulator is connected in this example with the V1 output supplying standby RAMs and the V2 output supplying a Z80 system. When V_i is removed the L4901's RESET output forces the RAMs into the standby state through the MC74HC138, which is also supplied from the backup battery

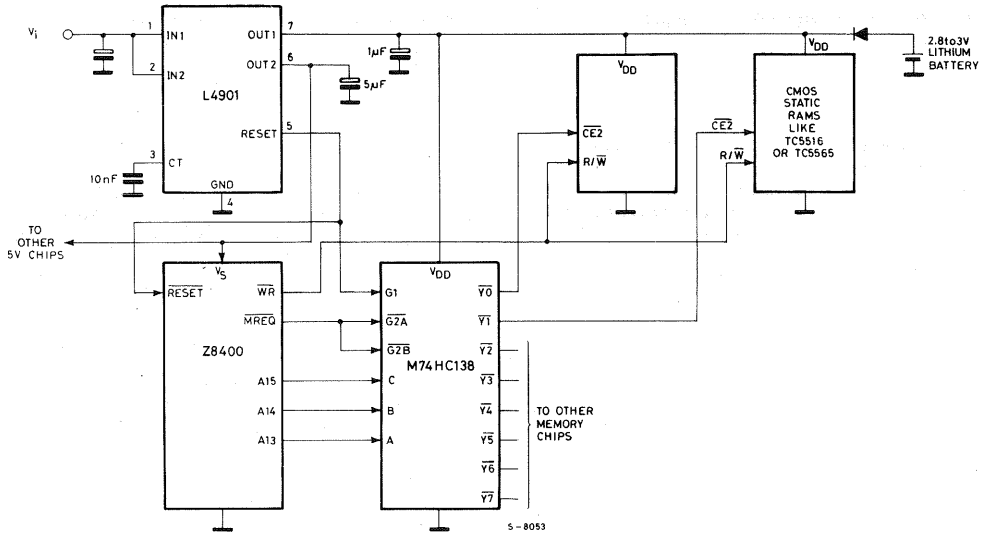
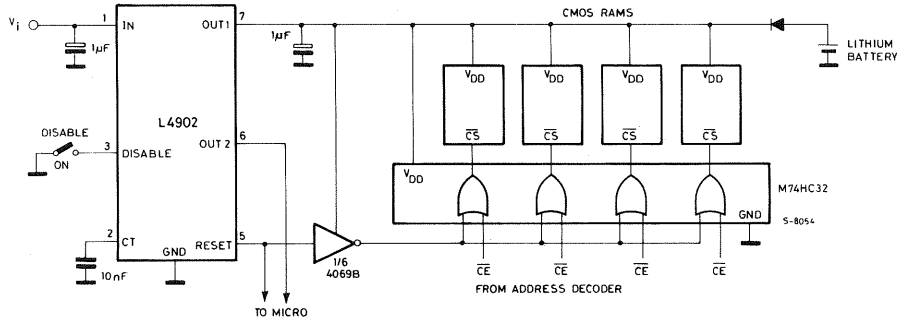
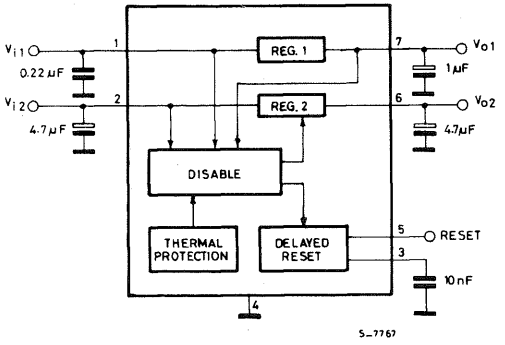


Fig. 3 - An alternative approach is to use OR gates to force the RAM's into standby mode. The L4902 used in this example has a disable input to switch the V2 output



An alternative, shown in figure 3, is to use OR gates to disable the RAMs when the supply is removed. This circuit also illustrates how the disables input of the L4902 turns off the V2 output. This disable input may be driven by an open-collector gate in applications where a standby or sleep-mode CMOS microcomputer turns off its ancillary circuits in the standby state.

Fig. 4 - Block diagram of the L4901 dual 5V regulator



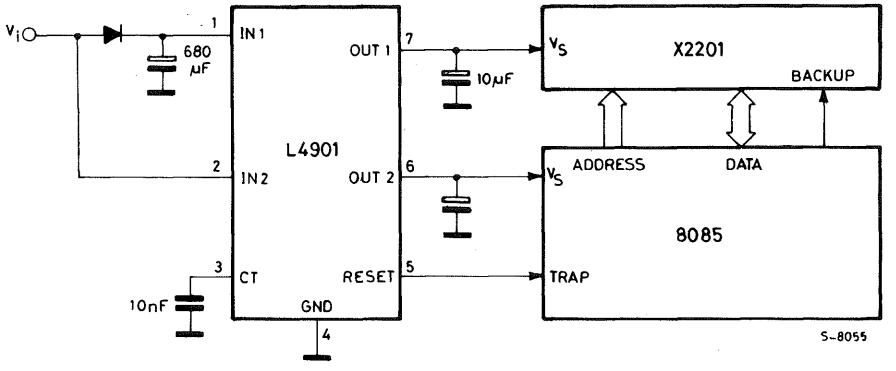
SHADOW-TYPE NV RAMs

In non-volative read/write memories like the XICOR X2201, where a fast volative RAM is backed-up by a slow EPROM, it is important to ensure that the backup command is generated when the supply is removed.

As shown in figure 5, this function can be performed by the RESET output of an L4901 dual regulator. A capacitor on the V1 input ensures that the X2201 is powered during the transfer operation.

When the input voltage is removed or goes below 6.3V, the L4901's reset output, connected to the 8085's TRAP input, forces the execution of a service routine which saves the state of the machine in the RAM then issues a backup command. The V2 output drops immediately while the 680µF capacitor on the V1 input provides enough energy to keep the X2201 running for the 10ms needed to complete the backup transfer. The low consumption of the V1 regulator allows the use of a relatively small capacitor for this function.

Fig. 5 - The L4901 is also useful for supplying shadow-type NVRAMs. In this circuit the RESET signal initiates a backup transfer. The 680µF capacitor on the V1 input provides enough energy to complete the transfer.



LOW DROP VOLTAGE REGULATORS FOR AUTOMOTIVE ELECTRONICS

Linear voltage regulators with an input-output voltage drop of less than 2V are used to ensure continuity of the stabilized output in applications where a battery supply is used. This note describes the characteristics and operation of these devices.

Low drop linear voltage regulators are low voltage (5 to 12V) regulators which are able to provide effective stabilization of the output voltage even when the difference between input voltage and output voltage is less than 2V.

This situation can arise accidentally for a brief period when the main supply source is overloaded. It may also result from a deliberate design decision aimed at reducing the power dissipated in the supply - for example, when the device is used as a post regulator in portable instruments.

Low drop regulators are used widely in automotive applications, a field where integrated circuits have to be particularly rugged. For this reason most low drop devices include protection functions not found in standard regulators. Before describing the SGS family of low drop regulators we will therefore begin with a brief description of the automotive electrical environment.

AUTOMOTIVE ENVIRONMENT

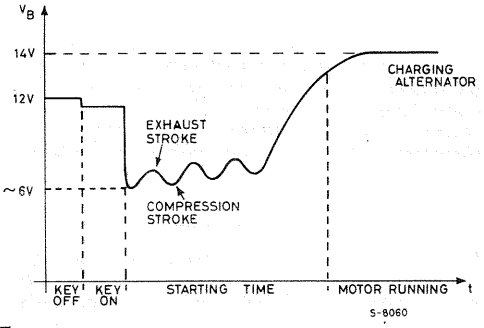
In addition to the battery voltage drop during starting, the automotive field presents a number of other serious problems concerning the regulator input voltage: positive and negative high energy/high voltage transients (load dump and field decay), positive e negative low energy/very-high-voltage spikes (switching spikes), battery reversal and battery voltage doubling.

All of these hazards must be withstood by the regulator without damage over an ambient temperature range very close to military standards (-40 to +125°C for underhood devices; -40 to +85°C for other devices). Moreover, an output voltage precision of ±4% to ±2% is required over the whole temperature range and in all conditions of input voltage and load current.

BATTERY VOLTAGE DROP

During motor starting the battery is overloaded by a peak current of up to 100A drawn by the starter motor. In this condition, which persists for 20-30ms, the battery voltage drops to about 6V in very cold weather (Figure 1).

Fig. 1 - Cold starting supply voltage drop



Using standard regulators with a dropout of 1.7V to 2.1V the minimum 4.75V supply necessary for essential functions such as ignition, injection and electronic engine control cannot be guaranteed. Another unfortunate consequence is the loss of RAM memory contents in car radios and trip computers.

A voltage regulator with a voltage drop of less than 1.2V is therefore necessary.

BATTERY VOLTAGE DOUBLING

To aid cold weather starting with a partially flat battery, sometimes two batteries are used in series, doubling the voltage. Regulators must therefore withstand input voltages of 24-26V without disturbing operation.

BATTERY REVERSAL

Voltage regulators must be protected internally against negative input voltages to guard against accidental battery reversal.

LOAD DUMP TRANSIENTS

Load dump transients are high voltage, high energy positive transients.

The response time of the output voltage of an alternator to load variations is very long because of the long time constant of the excitation winding and mechanical inertia.

When the load is reduced instantaneously (by turning off lights, cooling fans and so on) the output voltage of the alternator tends to present a positive peak, the amplitude of which depends on the speed of rotation and the excitation current.

During normal operation this does not cause problems because of the high capacity of the battery which, connected in parallel with the alternator output, is able to absorb the transient energy without a significant increase in voltage.

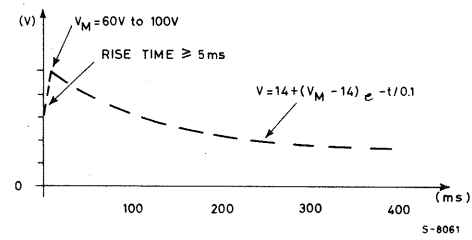
However, motor manufactures impose the standard that electronic devices must be protected against load dump transients because it is possible for the connection between battery and alternator to break.

The worst case voltage peak occurs when the battery-alternator cable is disconnected with the battery discharged and the motor running at its fastest rotation speed. In this case, the load variation is at a maximum and the voltage peak reaches a value comparable with the no-load output of the alternator running at maximum speed with the maximum excitation current.

Figure 2 shows a typical load dump waveform.

Motor manufacturers require that voltage regulators are able to protect themselves and the load against peak voltages of 60-100V with an equivalent series resistance of 0.1 to 1Ω, depending on the type of alternator and external protection device used.

Fig. 2 - Load dump transient



FIELD DECAY TRANSIENTS

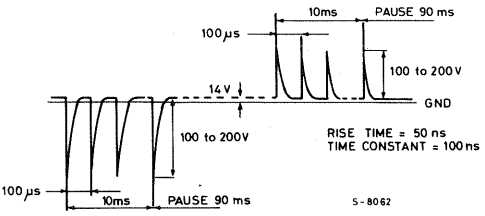
Field decay transients are high energy, high voltage negative transients.

If the ingition switch is turned off while current is flowing in inductive loads (electric motors, alternator field coil and so on) a negative voltage transient appears on the supply rail. The peak value in modulo of this transient is of the same order of magnitude as a load dump transient. In this case, too, the regulator must protect itself and the load.

SWITCHING SPIKES

Windscreen wiper motors, lamp flashers and ignition sparks behave as high frequency noise generators with an equivalent series resistance of 50 to 500Ω. The energy associated with these transients is much lower than load dump or field decay transients but the negative and positive peaks can reach 200V. Figure 3 shows the voltage waveform which the regulators must withstand.

Fig. 3 - Switching spikes



REGULATOR DESIGN

DROPOUT

The dropout voltage of a linear voltage regulator can be defined for a given output current, I_O, as the minimum difference between input and output voltage below which the output voltage is 100mV lower than the voltage measured at I_O with the

nominal input voltage. The current I_O must be specified since the dropout voltage increases as the load current increases.

To obtain a dropout voltage of 0.05 to 1V with an output current of 10 to 500mA, the regulator types L387, L487, L47XX, L48XX, L4920, L4921, LM2930A and LM2931A are configured with a PNP series-pass transistor as shown in figure 4. The PNP transistor is connected in the common emitter configuration and can therefore operate in saturation, yielding the low dropout voltage desired.

For higher dropout values an NPN series-pass element in emitter follower configuration may be used. This approach, shown in Figure 5, is used in the L2600 series regulators which have a maximum dropout voltage of 1.9V at 500mA.

Fig. 4 - PNP series pass transistor in common emitter configuration for very low drop out voltage regulators

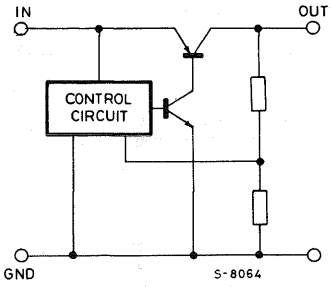
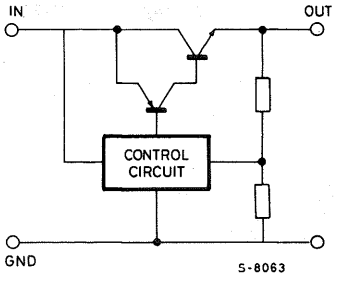


Fig. 5 - NPN series pass transistor in emitter follower configuration



CURRENT CONSUMPTION/QUIESCENT CURRENT

The circuit configurations shown in Figures 4 and 5 behave differently as far as concerns the current consumed by the device but not delivered to the load. In the case of figure 5, this current is that necessary for the functioning of the auxiliary circuitry of the regulator (voltage reference, op amp and so on). The base current of the output transistor flows into the load.

In the Figure 4 circuit, in contrast, the base current of the output transistor does not flow through the load and, particularly in saturation, depends heavily on the load current.

Normally lateral PNP transistors are chosen for ICs because they can withstand high positive and negative overvoltages. When negative overvoltages at the input do not occur, or are eliminated by external protection devices, vertical PNP transistors can be used in place of lateral types.

Since vertical PNP transistors have higher gain the current consumed in the regulator is significantly reduced. Vertical PNP transistors will be used in future designs.

VOLTAGE REFERENCE

The wide operating range of input voltage (6 to 26V) and ambient temperature (-40 to 125°C) over which high output voltage precision is required means that a well stabilized voltage reference must be used.

All SGS low drop regulators use bandgap type voltage references (see Figure 6). In this structure the two transistors Q_2 and Q_1 have an emitter area ratio of 10 and carry equal collector currents imposed by the current mirror Q_3, Q_4, Q_5. In these conditions the base-emitter voltages of Q_1 and Q_2 differ (at 25°C) by:

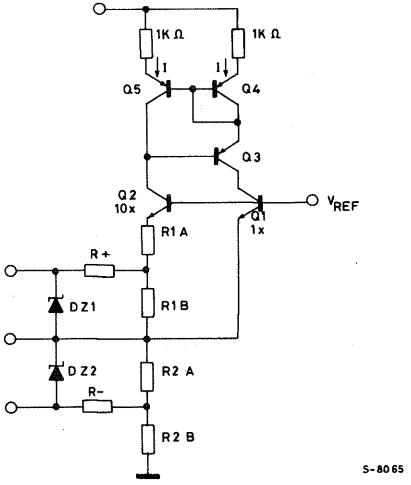
$$V_{BE} = \frac{KT}{q} \ln \frac{A(Q_2)}{A(Q_1)} = 60mV$$

where $\frac{A(Q_2)}{A(Q_1)} = 10$ (emitter area ratio)

$$\frac{KT}{q} = 26mV$$

K = Boltzmann's constant
T = Temperature in Kelvin
q = Charge on an electron

Fig. 6 - Bandgap voltage reference circuit in SGS low drop voltage regulators



The rejection of V_{ref} to variations in the supply voltage is improved by supplying the reference circuit from a stabilized voltage. This is achieved in the L26XX, L48XX, L4920, L4921, LM2930A and LM2931A regulators by means of a preregulator. In the L487, analysing the Figure 6 circuit gives:

$$V_{ref} = V_{BE}(Q_1) + 2\frac{R1}{R2}\Delta V_{BE}(Q_2, Q_1)$$

To maintain V_{ref} constant as temperature varies it is necessary that $\frac{d V_{ref}}{d T} = 0$ which implies choosing

$$\frac{R2}{R1} \text{ so that } \frac{2R2}{R1} \circ \frac{60}{T(25^\circ)} + \frac{d V_{BE}(Q_1)}{d T} = 0$$

where $T(25^\circ) = 298K$

$\frac{d V_{BE}(Q_1)}{d T}$ = negative temperature coefficient of the base-emitter voltage.

In L387 and L47XX regulators, in contrast, the supply to the bandgap is switched from the the input to the output as soon as the nominal output voltage is reached (Figures 7, 8, 9). The variation in output voltage with temperature is shown in Figure 10.

Fig. 7 - Block diagram of SGS L2600 series regulators

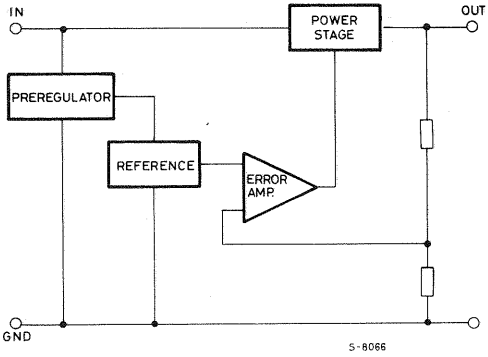


Fig. 8 - Block diagram of L387 L487 and L4700 series regulators

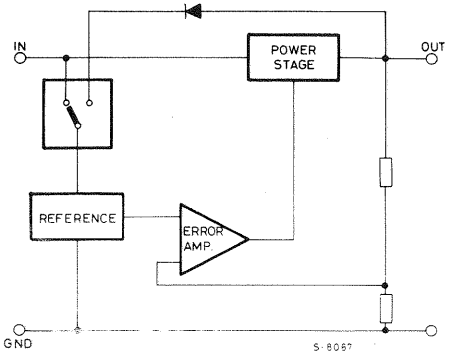


Fig. 9 - Block diagram of LM2930A, LM2931A, and L4800 series regulators

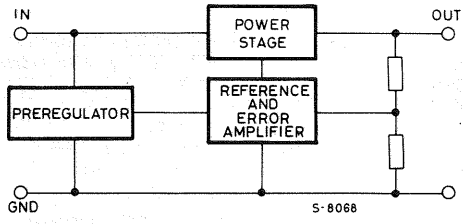
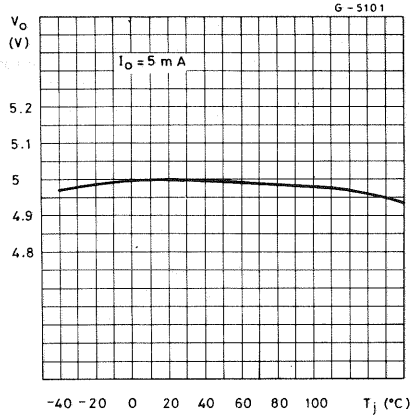


Fig. 10 - Output voltage vs. temperature



PROTECTION AGAINST HIGH ENERGY TRANSIENTS

To protect the LM2930A, LM2931A, L4920, L4921 and L48XX regulators against high-voltage, high-energy positive transients the basic circuit shown in Figure 11 is used. The zeners in this circuit limit the supply voltage to the maximum operating value and turn off the output stage. The output transistor can thus withstand voltages up to the BV_{CES} breakdown voltage.

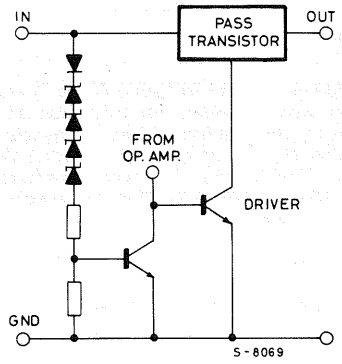
In the other regulators (L487, L387, L47XX and L26XX) the supply to the internal circuits is also turned off.

The speed of intervention of these protection schemes is fast enough to ensure that the regulator can withstand high energy transients with a rising slope of 10V/μs without problems, interrupting normal operation only momentarily.

Protection against negative transients is provided by the high series impedance of the possible current paths and the reverse BV_{BEO} breakdown voltage of the lateral PNP transistors (BV_{CBO}).

The breakdown voltages BV_{CES} and BV_{CBO} depend on the technology therefore the transient capability is ±60V, ±80V or ±100V for the various types.

Fig. 11 - Overvoltage protection circuit

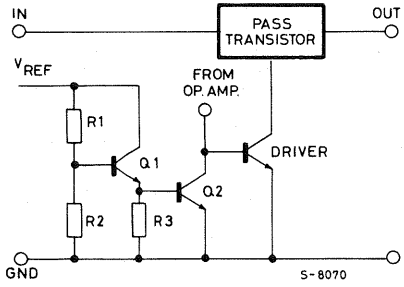


PROTECTION AGAINST LOW ENERGY OVERVOLTAGES

As shown in Figure 3, the low energy overvoltages which the devices must resist have very brief rise time and can exceed the breakdown voltages. The protection schemes described above are therefore insufficient. However, since the energy associated with these transients is very low, the regulators can withstand them without problems. Nevertheless it is advisable to place a capacitor of around 100nF at the input.

All of the SGS low drop regulators except the L26XX types need a compensation capacitor at the output. This capacitor also provides extra filtering for low energy transients because it has a low impedance at high frequencies.

Fig. 12 - Thermal protection circuit



THERMAL PROTECTION

When the junction temperature exceeds the safe maximum for the device a thermal protection circuit (Figure 12) holds the output transistor off until the overtemperature condition has passed.

In the Figure 12 circuit the resistors R1, R2 and R3 are calculated so that the base voltage of Q_1 is 600mV, thus preventing the conduction of Q_1 and Q_2.

As the junction temperature increases the minimum V_{BE} for conduction of the two transistors fall until, at about 15°C, $2V_{BE}$ = 600mV, the two transistors conduct and Q_2 turns off the output transistor driver.

CURRENT PROTECTION

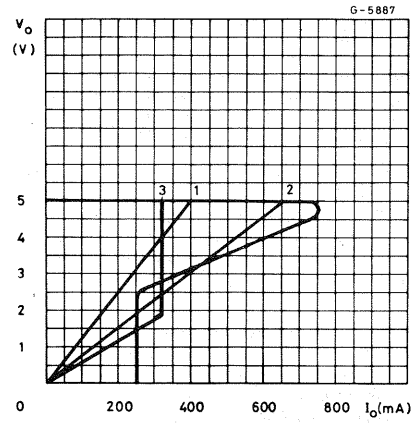
In the L487, L387 and L26XX regulators the output current is limited to its maximum value in the event of a short circuit. A special circuit acts on the base of the output transistor, preventing the output current from exceeding the limit set for the duration of the overload.

In the L4920, L4921, LM2930A, LM2931A and L48XX regulators a foldback circuit (Figure 13) is used to limit the power dissipated in both the devices and the load in short circuit conditions. The current is limited to a low value (I_{sc}) of about 200mA as soon as it exceeds the maximum value. The output voltage in this condition reaches a value corresponding to the current I_{sc} flowing through the load.

When the overload condition is removed the output voltage only returns to the nominal load value if the new static load line does not intersect the negative slope region of the curve in Figure 13. If it does, the new operating point will be at the intersection.

It is important to note that when power is applied, if the load line intersects the curve in the negative slope region, the regulator will operate with a lower-than-nominal voltage. This can happen with a passive load greater than the normal load (even if it is less than the maximum load I_M) or with active loads such as a current sinker which draw more than I_{sc} even at low voltages (Figure 13, curve 3).

Fig. 13 - 1) Acceptable load line for Turn-on
2) Unacceptable load line for Turn-on



EXTERNAL COMPENSATION

Since the purpose of a voltage regulator is to supply a fixed output voltage in spite of supply and load variations, the open loop gain of the regulator must be very high at low frequencies. This may cause instability as a result of the various poles present in the loop. To avoid this instability dominant pole compensation is used to reduce phase shifts due to other poles at the unity gain frequency. The lower the frequency of these other poles, the greater must be the capacitor used to create the dominant pole for the same DC gain.

Where the output transistor is a lateral PNP type there is a pole in the regulation loop at a frequency too low to be compensated by a capacitor which can be integrated. For the L487, L47XX, L48XX, L387, LM2930A and LM2931A external compensation is therefore necessary so a very high value capacitor must be connected from the output to ground.

The parassitic equivalent series resistance of the capacitor used adds a zero to the regulation loop. This zero may compromise the stability of the system since its effect tends to cancel the effect of the pole added. In SGS regulators this ESR must be less than 3Ω and the minimum capacitor value is 47μF. (100μF for L4800 series).

In the L2600, which uses an NPN power transistor, the stabilization capacitor is small enough to be integrated so no output capacitor is needed. Indeed, if an output capacitor is used it may cause oscillation unless it is greater than 100μF, in which case it would itself be the dominant pole. If an electrolytic capacitor of more than 100μF is used, a small capacitor must not be added in parallel or with the ESR of the electrolytic it would from another pole, worsening the stability of the system.

TURN-ON WITH CAPACITIVE LOADS

A load which presents a significant capacity between the output and ground (including the external compensation capacitor) will be seen by the regulator as a short circuit when power is applied. The regulator therefore delivers the short circuit current until the load capacitor has been charged to the nominal value.

This factor is extremely important for the dimensioning of the power source. Even a very small DC load can in such cases behave like a maximum load and the power drained from the supply is the sum of the short circuit current delivered to the load and the maximum current consumed in the regulator.

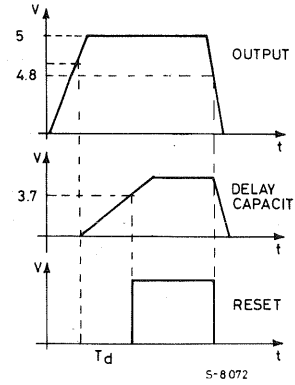
Moreover, as explained above, in regulators with foldback protection the static load line must not cross the negative slope region of Figure 13 or the output voltage will not reach the nominal value when power is applied.

SPECIAL FUNCTIONS

RESET

The L387 and L487 include a power on/off reset function which inhibits the operation of circuits supplied by the regulator when the output voltage is too low (4.75V) to guarantee correct operation of logic (Figure 14). To avoid malfunctions a delay is also introduced so that the enable signal is only issued some time after the safe output voltage has been reached.

Fig. 14 - Reset timing waveforms



The reset circuitry (Figure 15) consists of:

- a comparator connected between the voltage reference and a tap of the output divider, the voltage of which is higher than the feedback voltage;
- an SCR to memorize any brief glitches in the output voltage that can cause some trouble with the logic
- a delay circuit with an external capacitor charged by an internal current source

This function has been integrated into the voltage regulator to exploit the basic advantage of taking information at the source. The use of double calibrations can thus be avoided.

For the correct operation of the reset function, two basic relations must be satisfied in all cases

$$V_{resmax} < V_{outmin} \quad (1)$$

$$V_{resmin} > 4.75V \quad (2)$$

where $V_{res\,max}/V_{res\,min}$ are maximum/minimum value for the reset signal going high-low.

(1) means that the RESET signal must be high when the device is regulating

(2) means that the RESET signal must be low when the output voltage goes under 95% of

the nominal (5V). Expressions (1) and (2) can be rewritten as:

$(V_{resmax} - V_{resmin}) + (V_{nom} - V_{outmin}) <$ (3)

$< V_{nom} - 4.75V$

This means that the sum of all the errors in the worst case must be less than 5% (250mV).

- absolute spread of the reference
- error due to the load regulation (1% max)
- error due to the offset of the reset comparator and error amplifier (0.5%)
- errors due to the output divider (0.5%)
- hysteresis of the comparator to speed up the transitions (50mV that is 1% referred to 5V output)

VARIABLE OUTPUT VOLTAGE

The L4920 and L4921 are structurally identical to L48XX series regulators except that the voltage divider in the feedback loop is available externally (Figure 16). The output voltage can therefore be varied from 1.25V (the reference voltage) to 20V. It should be noted, however, that the minimum input voltage is 5.1V for operation with output voltages below 4.5V (otherwise the internal circuits will not work). For output voltages above 4.5V the input voltage must be at least equal to the output voltage plus the dropout voltage. The L4920 and L4921 are therefore low dropout regulators only for voltages above 4.5V.

A value of 6KΩ is recommended for R2 to match the internal circuitry.

Fig. 15 - Schematic block diagram of a voltage regulator with reset function

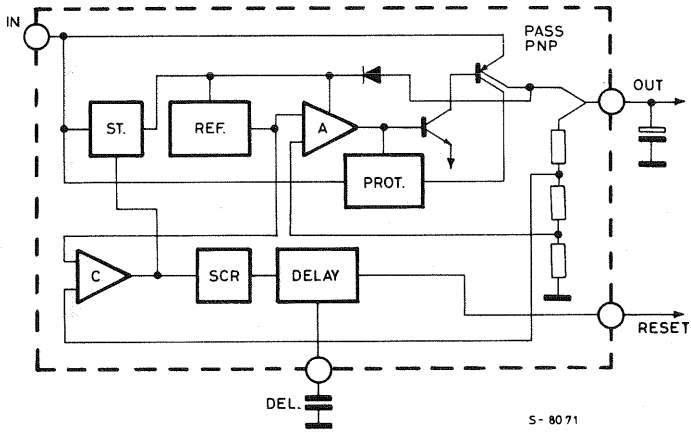
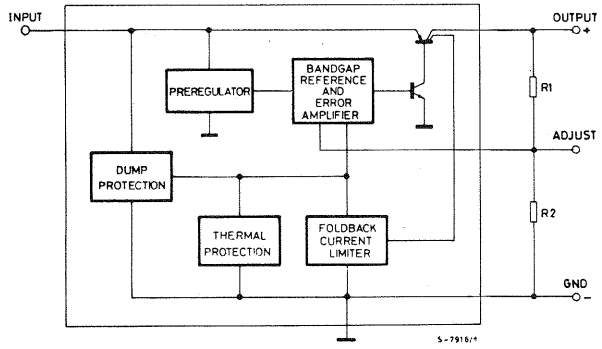


Fig. 16 - The L4920 and L4921 are structurally identical to L48XX series regulators except that the voltage divider in the feedback loop is available externally.



A DESIGNER'S GUIDE TO THE L200 VOLTAGE REGULATOR

Delivering 2A at a voltage variable from 2.85V to 36V, the L200 voltage regulator is a versatile device that simplifies the design of linear supplies. This design guide describes the operation of the device and its applications.

The introduction of integrated regulator circuits has greatly simplified the work involved in designing supplies. Regulation and protection circuits required for the supply, previously realized using discrete components, are now integrated in a single chip. This has led to significant cost and space saving as well as increased reliability. Today the designer has a wide range of fixed and adjustable, positive and negative series regulators to choose from as well as an increasing number of switching regulators.

The L200 is a positive variable voltage regulator which includes a current limiter and supplies up to 2A at 2.85 to 36V.

The output voltage is fixed with two resistors or, if a continuously variable output voltage is required, with one fixed and one variable resistor.

The maximum output current is fixed with a low value resistor. The device has all the characteristics common to normal fixed regulators and these are described in the datasheet. The L200 is particularly suitable for applications requiring output voltage variation or when a voltage not provided by the standard regulators is required or when a special limit must be placed on the output current.

The L200 is available in two packages:

Pentawatt — Offers easy assembly and good reliability. The guaranteed thermal resistance ($R_{th\ j\text{-}case}$) is 3°C/W (typically 2°C/W) while if the device is used without heatsink we can consider a guaranteed junction-ambient thermal resistance of 50°C/W.

TO-3 — For professional and military use or where good hermeticity is required.
The guaranteed junction-case thermal resistance is 4°C/W, while the junction-ambient thermal resistance is 35°C/W.

The junction-case thermal resistance of this package, which is greater than that of the Pentawatt, is partly compensated by the lower contact resistance with the heatsink, especially when an electrical insulator is used.

CIRCUIT OPERATION

As can be seen from the block diagram (fig. 1) the voltage regulation loop is almost identical to that of fixed regulators. The only difference is that the negative feedback network is external, so it can be varied (fig. 3). The output is linked to the reference by:

$$V_{out} = V_{ref} \left(1 + \frac{R2}{R1}\right) \qquad (1)$$

Considering V_{out} as the output of an operational amplifier with gain equal to $G_v = 1 + R2/R1$ and input signal equal to V_{ref}, variability of the output voltage can be obtained by varying R1 or R2 (or both). It's best to vary R1 because in this way the current in resistors R1 and R2 remains constant (this current is in fact given by $V_{ref}/R1$).

(Equation (1) can also be found in another way which is more useful in order to understand the descriptions of the applications discussed.

$$V_{out} = R1\ i_1 + R2\ i_2$$

and since in practice $i_1 \gg i_4$ (i_4 has a typical value of 10 μA) we can say that

$$V_{out} = R1\ i_1 + R2\ i_1 \quad \text{with} \quad i_1 = \frac{V_{ref}}{R1}$$

Therefore

$$V_{out} = \frac{R2}{R1} V_{ref} + V_{ref} = V_{ref} \left(1 + \frac{R2}{R1}\right)$$

In other words R1 fixes the value of the current circulating in R2 so R2 is determined.

Fig. 1 - Block diagram

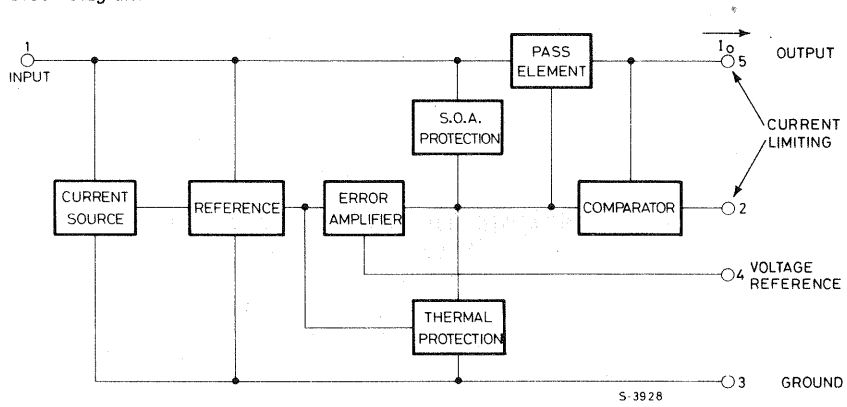


Fig. 2 - Schematic diagram

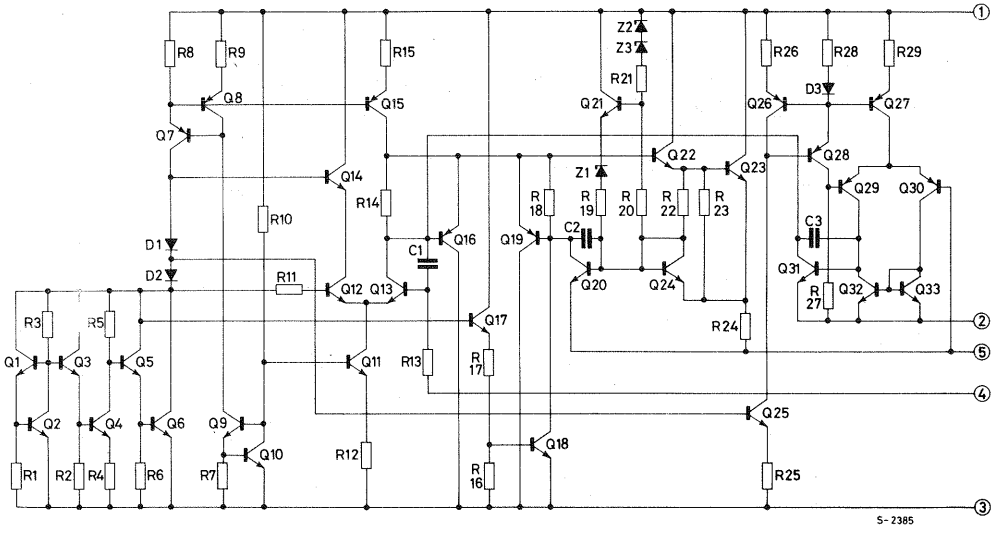
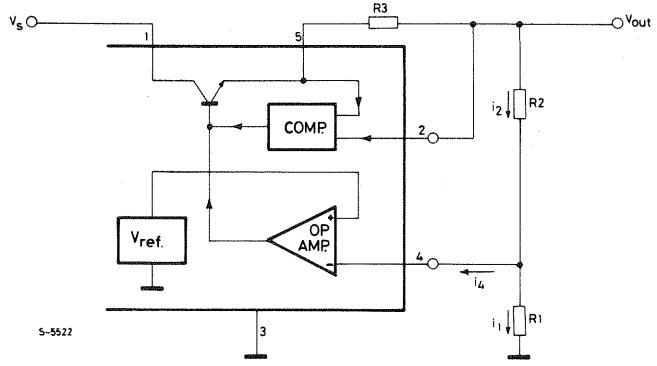


Fig. 3

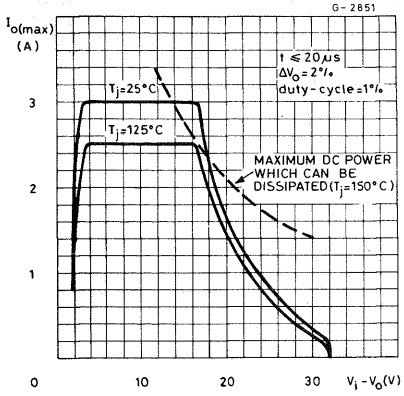


Overload protection

The device has an overload protection circuit which limits the current available.

Referring to fig. 2, R24 operates as a current sensor. When at the terminals of R24 there is a voltage drop sufficient to make Q20 conduct, Q19 begins to draw current from the base of the power transistor (darlington formed by Q22 and Q23) and the output current is limited. The limit depends on the current which Q21 injects into the base of Q20. This current depends on the drop-out and the temperature which explains the trend of the curves in fig. 4.

Fig. 4



Thermal protection

The junction temperature of the device may reach destructive levels during a short circuit at the output or due to an abnormal increase in the ambient temperature. To avoid having to use heatsinks which are costly and bulky, a thermal protection circuit has been introduced to limit the output current so that the dissipated power does not bring the junction temperature above the values allowed. The operation of this circuit can be summarized as follows.

In Q17 there is a constant current equal to:

$$\frac{V_{ref} - V_{BE17}}{R17 + R16} \qquad (V_{ref} = 2.75V \text{ typ})$$

The base of Q18 is therefore biased at:

$$V_{BE18} = \frac{V_{ref} - V_{BE17}}{R16 + R17} \cdot R16 \cong 350 \text{ mV}$$

Therefore at T_j = 25°C Q18 is off (since 600 mV is needed for it to start conducting). Since the V_{BE} of a silicon transistor decreases by about 2 mV/°C, Q18 starts conducting at the junction temperature:

$$T_j = \frac{600-350}{2} + 25 = 150°C$$

Current limitation

The innovative feature of this device is the possibility of acting on the current regulation loop, i.e. of limiting the maximum current that can be supplied to the desired value by using a simple resistor (R3 in fig. 2). Obviously if R3 = 0 the maximum output current is also the maximum current that the device can supply because of its internal limitation.

The current loop consists of a comparator circuit with fixed threshold whose value is V_{sc}. This comparator intervenes when $I_o \cdot R3 = V_{sc}$, hence $I_o = \frac{V_{sc}}{R3}$ (V_{sc} is the voltage between pins 5 and 2 with typical value of 0.45V).

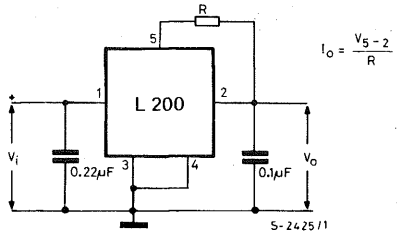
Special attention has been given to the comparator circuit in order to ensure that the device behaves as a current generator with high output impedance.

TYPICAL APPLICATIONS

Programmable current regulator

Fig. 5 shows the device used as current generator. In this case the error amplifier is disabled by short-circuiting pin 4 to ground.

Fig. 5



The output current I_o is fixed by means of R:

$$I_o = \frac{V_{5-2}}{R}$$

The output voltage can reach a maximum value $V_i - V_{drop} \cong V_i - 2V$ (V_{drop} depends on I_o).

Programmable voltage regulator

Fig. 6 shows the device connected as a voltage regulator and the maximum output current is the maximum current that the device can supply. The output voltage V_o is fixed using potentiometer R2. The equation which gives the output voltage is as follows:

$$V_o = V_{ref}\left(1 + \frac{R2}{R1}\right)$$

By substituting the potentiometer with a fixed resistor and choosing suitable values for R1 and R2, it is possible to obtain a wide range of fixed output voltages.

Fig. 6

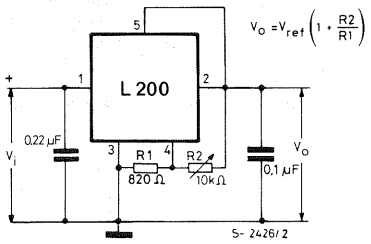
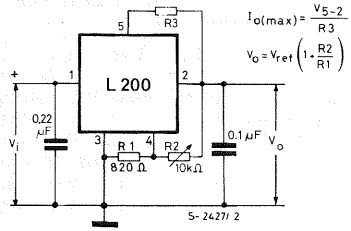


Fig. 7



The following formulas and tables can be used to calculate some of the most common output voltages.

Having fixed a certain V_o, using the previous formula, the maximum value is:

$$V_{o\ max} = V_{ref\ max}\ (1 + \frac{R2\ max}{R1_{min}})$$ and the minimum value is:

$$V_{o\ min} = V_{ref\ min}\ (1 + \frac{R2\ min}{R1\ max})$$

The table below indicates resistor values for typical output voltages:

V_o ± 4%	R1 ± 1%	R2 ± 1%
5V	1.5 kΩ	1.2 kΩ
12V	1 kΩ	3.3 kΩ
15V	750 Ω	3.3 kΩ
18V	330 Ω	1.8 kΩ
24V	510 Ω	3.9 kΩ

Programmable current and voltage regulator

The typical configuration used by the device as a voltage regulator with external current limitation is shown in fig. 7. The fixed voltage of 2.77V at the terminals of R1 makes it possible to force a constant current across variable resistor R2. If R2 is varied, the voltage at pin 2 is varied and so is the output voltage.

The output voltage is given by:

$$V_o = V_{ref} \cdot (1 + \frac{R2}{R1}),\ \text{with}\ V_{ref} = 2.77V\ \text{typ}$$

and the maximum output current is given by:

$$I_{o\ max} = \frac{V_{5-2}}{R3}\ \text{with}\ V_{5-2} = 0.45V\ \text{typ.}$$

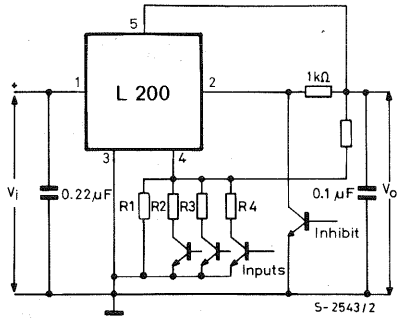
To maintain a sufficient current for good regulation the value of R1 should be kept low. When there is no load, the output current is $V_{ref}/R1$. Suitable values of R1 are between 500Ω and 1.5 kΩ. If the load is always present the maximum value for R1 is limited by the current value (10 µA) at the input of the error amplifier (pin 4).

Digitally selected regulator with inhibit

The output voltage of the device can be regulated digitally as shown in fig. 8. The output voltage depends on the divider formed by R5 and a combination of R1, R2, R3 and P2. The device can be switched off with a transistor.

When the inhibit transistor is saturated, pin 2 is brought to ground potential and the output voltage does not exceed 0.45V.

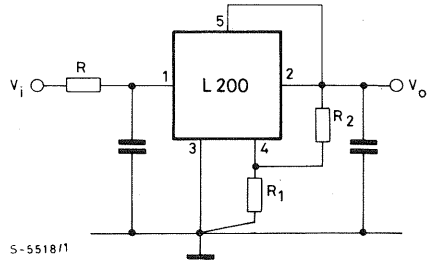
Fig. 8



Reducing power dissipation with dropping resistor

If may sometimes be advisable to reduce the power dissipated by the device. A simple and economic method of doing this is to use a resistor connected in series to the input as shown in fig. 9. The input-output differential voltage on the device is thus reduced.

Fig. 9



The formula for calculating R is as follows:

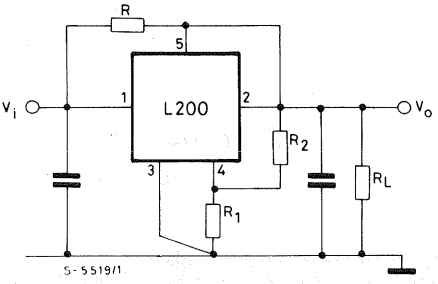
$$R = \frac{V_{i\,min} - (V_o + V_{drop})}{I_o}$$

Where V_{drop} is the minimum differential voltage between the input and the output of the device at current I_o. $V_{in\,min}$ is the minimum input voltage. V_o is the output voltage and I_o the output current.

With constant load, resistor R can be connected between pins 1 and 2 of the IC instead of in series with the input (fig. 10). In this way, part of the load current flows through the device and part through the resistor. This configuration can be used when the minimum current by the load is:

$$I_{o\,min} = \frac{V_{drop}}{R} \quad \text{(instant by instant)}$$

Fig. 10



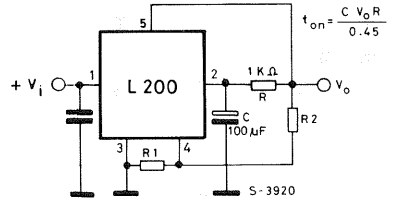
Soft start

When a slow rise time of the output voltage is required, the configuration in fig. 11 can be used. The rise time can be found using the following formula:

$$t_{on} = \frac{CVo\,R}{0.45}$$

At switch on capacitor C is discharged and it keeps the voltage at pin 2 low; or rather, since a voltage of more than 0.45V cannot be generated between pins 5 and 2, the V_o follows the voltage at pin 2 at less than 0.45V.

Fig. 11



Capacitor C is charged by the constant current i_c.

$$i_c = \frac{V_{sc}}{R}$$

Therefore the output reaches its nominal value after the time t_{on}:

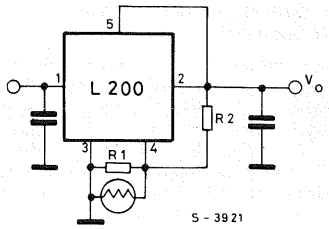
$$V_o - V_{sc} = \frac{i_c \cdot t_{on}}{C}$$

$$t_{on} = C \cdot \frac{(V_o - 0.45)}{0.45} \cdot R \cong \frac{CV_o\,R}{0.45}$$

Light controller

Fig. 12 shows a circuit in which the output voltage is controlled by the brightness of the surrounding environment. Regulation is by means of a photoresistor in parallel with R1. In this case, the output voltage increases as the brightness increases. The opposite effect, i.e. dimming the light as the ambient light increases, can be obtained by connecting the photoresistor in parallel with R2.

Fig. 12



Light dimmer for car display

Although digital displays in cars are often more aesthetically pleasing and frequently more easily read they do have a problem. Under varying ambient light conditions they are either lost in the background or alternatively appear so bright as to distract the driver. With the system proposed here, this problem is overcome by automatically adjusting the display brightness during daylight conditions and by giving the driver control over the brightness during dusk and darkness conditions.

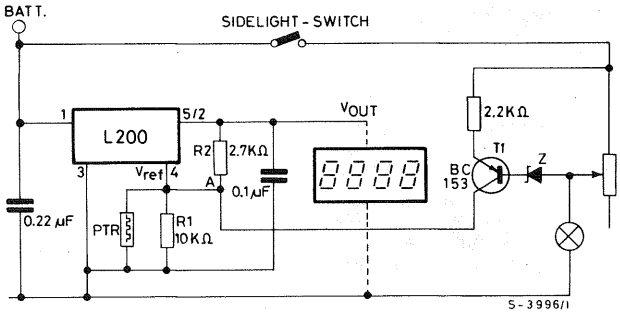
The circuit is shown in fig. 13. The primary supply is shown taken straight from the car battery however it is worth noting that in a car there is always the risk of dump voltages up to 120V and it is recommended that some form of protection is included against this.

Under daylight conditions i.e. with sidelights off and T1 not conducting the output of the device is determined by the values of R1, R2 and the photoresitor (PTR). The output voltage is given by

$$V_{out} = V_{ref}\,(1 + \frac{R2}{PTR//R1})$$

If the ambient light intensity is high, the resistance of the photoresistor will be low and therefore V_{out} will be high. As the light decreases, so V_{out} decreases dimming the display to a suitable level.

Fig. 13



In dusk conditions, when the sidelights are switched on, T1 starts to conduct with its conduction set by the potentiometer. With the potentiometer wiper at its uppermost position the sidelights are at their brightest and current through T1 would be a minimum. With the wiper at its lowest position obviously the opposite conditions apply.

The current through T1 is felt at the summing node A along with the currents through R2 and the parallel network R1, PTR. Since V_{ref} is constant the current flowing through R1, PTR must also be constant. Therefore any change in the current through T1 causes an equal and opposite change in the current through R2. Therefore as I_{T1} increases, V_{out} decreases i.e. as the brightness of the sidelights is increased or decreased so is the brightness of the display.

The values of R2 and PTR should be selected to give the desired minimum and maximum brightness levels desired under both automatic and manual conditions although the minimum brightness under manual conditions can also be set by the maximum current flowing through T1 and, in any case, this should not exceed the maximum current through R2 under automatic operation.

The circuit shown with a small modification can also be used for dimmers other than in a car. Fig. 15 shows the modification needed. The zener diode should have a $V_F \geqslant 2.5V$ at $I = 10\ \mu A$.

Fig. 14

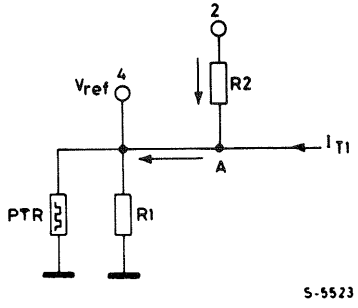
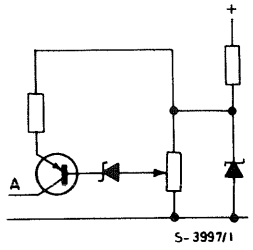


Fig. 15



Higher input or output voltages

Certain applications may require higher input or output voltages than the device can produce. The problem can be solved by bringing the regulator back into the normal operating units with the help of external components.

When there are high input voltages, the excess voltage must be absorbed with a transistor. Figs. 16 and 17 show the two circuits:

Fig. 16

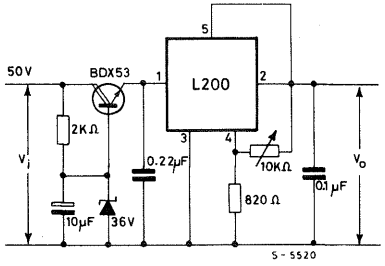
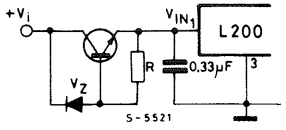


Fig. 17



The designer must take into account the dissipated power and the SOA of the preregulation transistor. For example, using the BDX53, the maximum input voltage can reach 56V (fig. 16). In these conditions we have 20V of V_{CE} on the transistor and with a load current of 2A the operation point remains inside the SOA. The preregulation used in fig. 16 reduces the ripple at the input of the device, making it possible to obtain an output voltage with negligible ripple.

If high output voltages are also required, a second zener, V_z, is used to refer the ground pin of an IC to a potential other than zero; diode D1 provides output shortcircuit protection (fig. 18).

Fig. 18

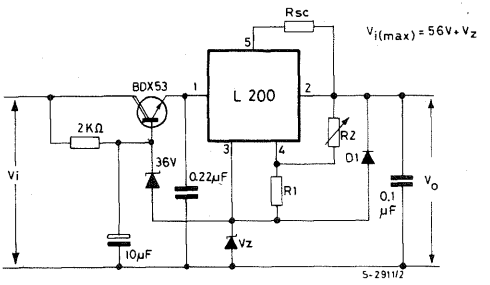
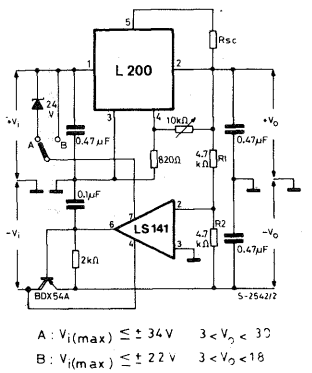


Fig. 19



A : $V_{i(max)} \leq \pm 34V$ $3 < V_o < 30$

B : $V_{i(max)} \leq \pm 22V$ $3 < V_o < 18$

Positive and negative voltage regulators

The circuit in fig. 19 provides positive and negative balanced, stabilized voltages simultaneously. The L200 regulator supplies the positive voltage while the negative is obtained using an operational amplifier connected as follower with output current booster.

Tracking of the positive voltage is achieved by putting the non-inverting input to ground and using the inverting input to measure the feedback voltage coming from divider R1-R2.

The system is balanced when the inputs of the operational amplifier are at the same voltage, or, since one input is at fixed ground potential, when the voltage of the intermediate point of the divider goes to 0 Volts. This is only possible if the negative voltage, on command of the op-amp, goes to a value which will make a current equal to that in R1 flows in R2. The ratio which expresses the negative output voltage is:

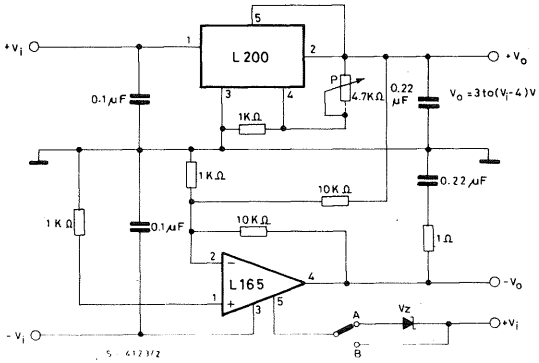
$$V^- = V^+ \cdot \frac{R2}{R1} \qquad \text{(If R2= R1, we'll get } V^- = V^+\text{)}$$

Since the maximum supply voltage of the op amp used is ± 22V, when pin 7 is connected to point B output voltages up to about 18V can be obtained. If on the other hand pin 7 is connected to point A, much higher output voltages, up to about 30V, be obtained since in this case the input voltage can rise to 34V.

Fig. 20 shows a diagram is which the L165 power op amp is used to produce the negative voltage. In this case (as in fig. 19) the output voltage is limited by the absolute maximum rating of the supply voltage of the L165 which is ± 18V. Therefore to get a higher V_{out} we must use a zener to keep the device supply within the safety limits.

If we have a transformer with two separate secondaries, the diagram of fig. 21 can be used to obtain independent positive and negative voltages. The two output diodes, D1 and D2, protect the devices from shortcircuits between the positive and negative outputs.

Fig. 20



A: for $\pm 18V \leq V_i \leq 32V$

Note: V_z must be chosen in order to verify $2V_i - V_z = 36V$

B: for $V_i \leq \pm 18V$

Fig. 21

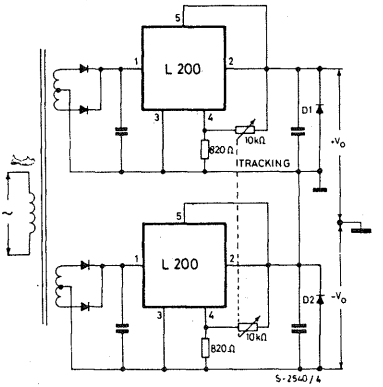
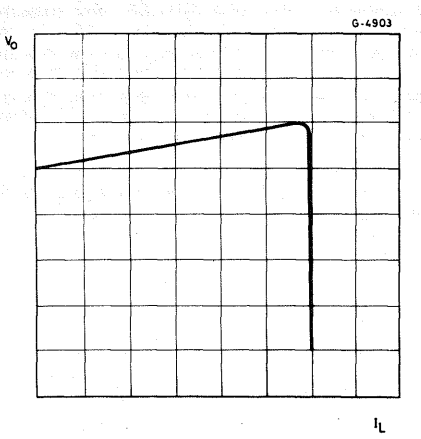


Fig. 23



Compensation of voltage drop along the wires

The diagram in fig. 22 is particularly suitable when a load situated far from the output of the regulator has to be supplied and when we want to avoid the use of two sensing wires. In fact, it is possible to compensate the voltage drop on the line caused by the load current (see the two curves in fig. 23 and 24). R_K transforms the load current I_L into a proportional voltage in series to the reference of the L200. R_K I_L is then amplified by the factor

$$\frac{R2 + R1}{R1}.$$

With the values of R_Z, R2 and R1 known, we get:

$$R_K = R_Z \frac{R1}{R1 + R2}$$

R_Z, R1 and R2 are assumed to be constant.
If R_K is higher than 10 Ω, the output voltage should be calculated as follows:

$$V_o = I_d \, R_K + V_{ref} \frac{R2 + R1}{R1}$$

Fig. 24

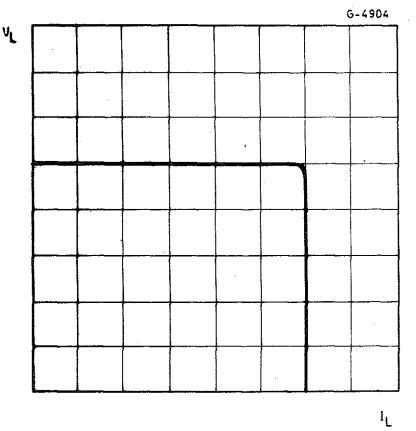
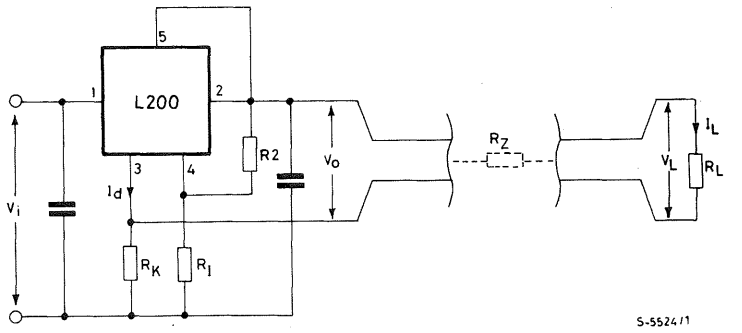


Fig. 22



Motor speed control

Fig. 25 shows how to use the device for the speed control of permanent magnet motors. The desired speed, proportional to the voltage at the terminal of the motor, is obtained by means of R1 and R2.

$$V_M = V_{ref}\left(1 + \frac{R2}{R1}\right)$$

To obtain better compensation of the internal motor resistance, which is essential for good regulation, the following equation is used:

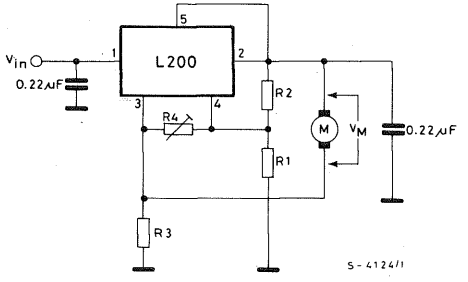
$$R3 \leqslant \frac{R1}{R2} \cdot R_M$$

This equation works with infinite R4. If R4 is finite, the motor speed can be increased without altering the ratio R2/R1 and R3. Since R4 has a constant voltage (V_{ref}) at its terminals, which does not vary as R4 varies, this voltage acts on R2 as a constant current source variable with R4. The voltage drop on R2 thus increases, and the increase is felt by the voltage at the terminals of the motor. The voltage increase at the motor terminals is:

$$V_M = \frac{V_{ref}}{R4 + R3} \cdot R2.$$

A circuit for a 30W motor with $R_M = 4\Omega$, $R1 \doteq 1\,k\Omega$, R2 = 4.3 kΩ, R4 = 22 kΩ and R3 = 0.82Ω has been realized.

Fig. 25



Power amplitude modulator

In the configuration of fig. 26 the L200 is used to send a signal onto a supply line. Since the input signal V_i is DC decoupled, the V_o is defined by:

$$V_o = V_{ref}\left(1 + \frac{R2}{R1}\right)$$

The amplified signal V_i whose value is:

$$G_v = -\frac{R2}{R3}$$

is added to this component. By ignoring the current entering pin 4, we must impose $i_1 = i_2 + i_3$ (1) and since the voltage between pin 4 and ground remains fixed (V_{ref}) as long as the device is not in saturation, $i_1 = 0$ and equation (1) becomes:

$$i_2 = -i_3 \text{ with } i_3 = \frac{V_i}{R3} \text{ (for } X_C \ll R3\text{) - Therefore:}$$

$$V_o = R2\ i_2 = -\frac{V_i}{R3} \cdot R2.$$

An application is shown in fig. 27. If the DC level is to be varied but not the AC gain, R1 should be replaced by a potentiometer.

Fig. 26

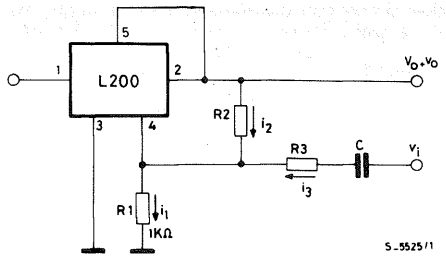
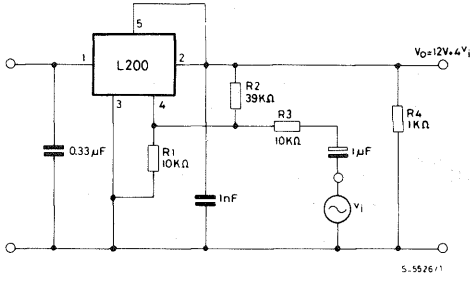


Fig. 27



HIGH CURRENT REGULATORS

To get a higher current than can be supplied by a single device one or more external power transistors must be introduced. The problem is then to extend all the device's protection circuits (short-circuit protection, limitation of T_j of external power devices and overload protection) to the external transistors. Constant current or foldback current limitation therefore becomes necessary.

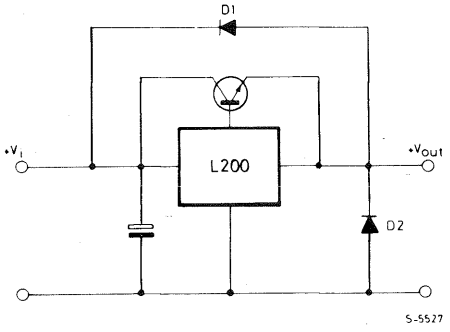
When the regulator is expected to withstand a permanent shortcircuit, constant current limitation becomes more and more difficult to guarantee as the nominal V_o increases. This is because of the increase in V_{CE} at the terminals of the transistor, which leads to an increase in the dissipated power. The heatsink has to be calculated in the heaviest working conditions, and therefore in shortcircuit. This increases weight, volume and cost of the heatsink and increase of the ambient temperature (because of high power dissipation). Besides heatsink, power transistors must be dimensioned for the short-circuit.

This type, of limitation is suited, for example, with highly capacitive loads. Efficiency is increased if preregulation is used on the input voltage to maintain a constant drop-out on the power element for all V_{out}, even in shortcircuit. Foldback limitation, on the other hand, allows lighter short-circuit operating conditions than the previous case. The type of load is important.

If the load is highly capacitive, it is not possible to have a high ratio between I_{max} and I_{sc} because at switch-on, with load inserted, the output may not reach its nominal value.

Other protection against input shortcircuit, mains failure, overvoltages and output reverse bias can be realized using two diodes, D1 and D2, inserted as indicated in fig. 28.

Fig. 28



Use of a PNP power transistor

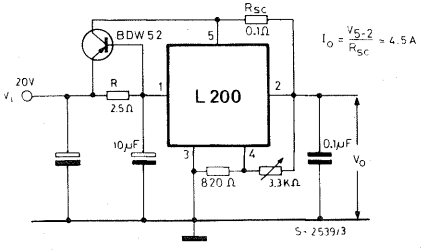
Fig. 29 shows the diagram of a high current supply using the current limitation of the L200. The output current is calculated using the following formula:

$$I_o = \frac{V_{SC}}{R_{SC}} \cong \frac{0.45V}{0.1\Omega} = 4.5A$$

Constant current limitation is used; so, in output shortcircuit conditions, the transistor dissipates a power equal to:

$$PD = V_i \cdot I_o = V_i \cdot \frac{V_{SC}}{R_{SC}}$$

Fig. 29



The operating point of the transistor should be kept well within the SOA; with R_{SC}= 0.1Ω, V_i must not exceed 20V. Part of the I_o crosses the transistor and part crosses the regulator.

The latter is given by: $I_{REG} = I_B + \frac{V_{BE}}{R}$.

where I_B is the base current of the transistor (-100 mA at I_C= 4A) and V_{BE} is the base-emitter voltage (-1V at I_C = 4A); with R = 2.5Ω, $I_{REG} \cong$ ≅ 500 mA.

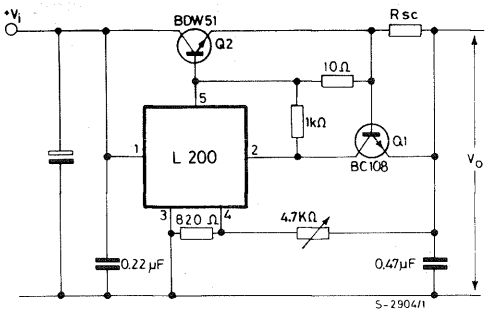
Use of an NPN power transistor

Fig. 30 shows the same application as described in figure 29, using an NPN power transistor instead of a PNP. In this case an external signal transistor must be used to limit the current. Therefore:

$$I_o = \frac{V_{BE\ Q1}}{R_{SC}}$$

As regards the output shortcircuit, see par. 1.5.

Fig. 30



12V 4A Power supply

The diagram in fig. 31 shows a supply using the L200 and the BD705. The 1 kΩ potentiometer, PT1, together with the 3.3 kΩ resistor are used for fine regulation of the output voltage.

Current limitation is of the type shown in fig. 32. Trimmer PT2 acts on strech AB of characteristic. With the values indicated (PT2= 1 kΩ, PT3= 470Ω, R = 3 kΩ), currents from 3 to 4A can be limited. The field of variation can be increased by increasing the value of R_{SC} or by connecting one terminal of PT3 to the base of the power transistor, which, however, provides less stable limitation. If section AB is moved, section BC will also be moved.

The slope of BC can be varied using PT3. The voltage level at point B is fixed by the voltage of the zener diode. The capacitor in parallel to the zener ensures correct switch-on with full load. The BD705 should always be used well within its safe operating area. If this is not possible two or more BD705s should be used, connected in parallel (fig. 33).

Further protection for the external power transistor can be provided as shown in fig. 34. The PTC resistor, whose temperature intervention point must prevent the T_j of the power transistor from reaching its maximum value, should be fixed to the dissipator near the power transistor. Dimensioning of R_A and R_B depends on the PTC used.

Fig. 31

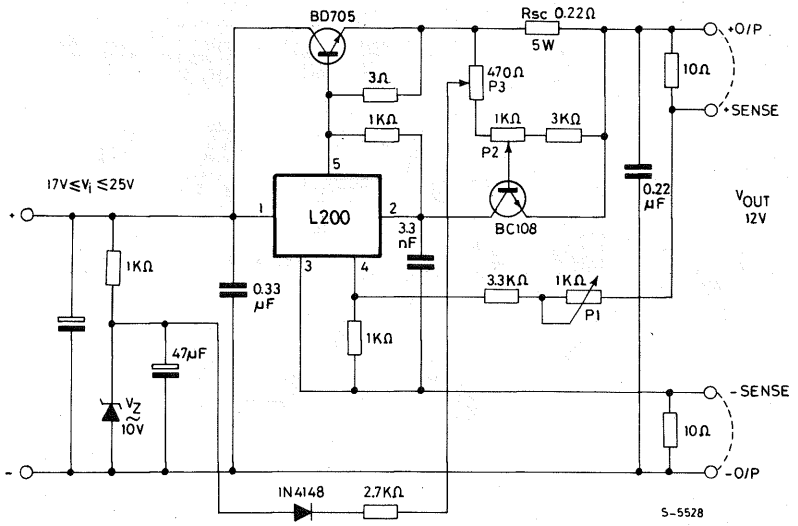


Fig. 32

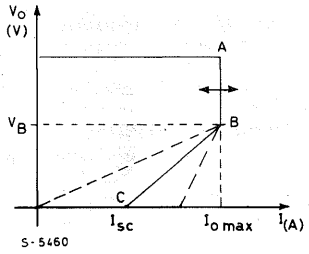


Fig. 34

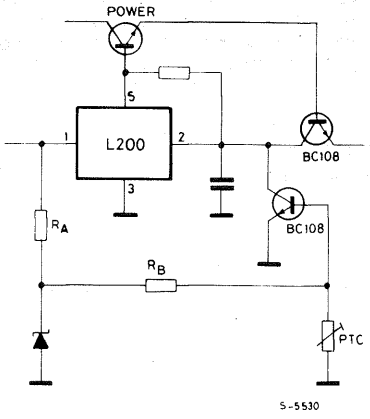
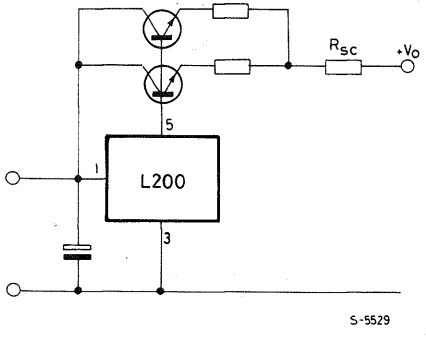


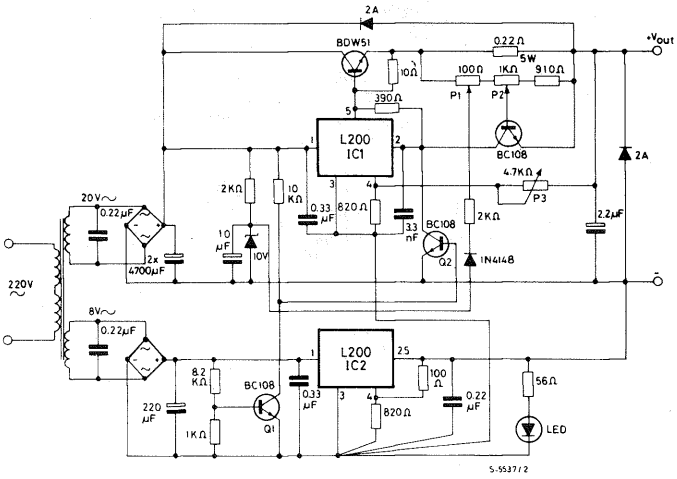
Fig. 33



Voltage regulator from 0V to 16V - 4.5A

Fig. 35 shows an application for a high current supply with output voltage adjustable from 0V to 16V, realized with two L200 regulators and an external power transistor. With the values indicated, the current can be regulated from 2A to 4.5A by potentiometer PT2. PT1, on the other hand, is used for constant current or foldback current limitation. The integrated circuit IC2, which does not require a heatsink and has excellent temperature stability, is used to obtain the 0V output. It is connected so as to lower pin 3 of IC1 until pin 4 reaches 0V. Q1 and Q2 ensure correct operation of the supply at switch-on and switch-off.

Fig. 35



Power supply with V_o= 2.8 to 18V, I_o= 0 to 2.5A

The diagram in fig. 36 shows a supply with output voltage variable from 2.8V to 18V and constant current limitation from 0A to 2.5A. The output current can be regulated over a wide range by means of the op. amp. and signal transistor TR_2. The op. amp. and the transistor are connected in the voltage-current converter configuration. The voltage is taken at the terminals of R3 and converted into current by PT_2.

I_o is fixed as follows:

$$\frac{R4\ I_o}{PT_2} = I_1\ (*) \qquad (**)\ I_{sc} = \frac{V_{SC}}{R2}$$

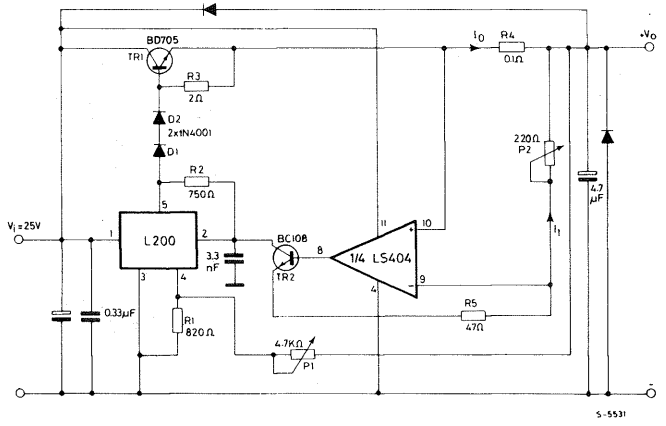
When $I_1 = I_{sc}$, the regulator starts to operate as a current generator. By making (*) equal to (**) we get:

$$\frac{R4\ I_o}{PT_2} = \frac{V_{SC}}{R2}\ ;\ \text{therefore}\ I_o = \frac{V_{SC}}{R2 \cdot R4} \cdot PT_2.$$

Diodes D1 and D2 keep transistor TR_2 in linear condition in the case of small output currents. If it is not necessary to limit the current to zero, one of the diodes can be eliminated: the second diode could also be eliminated if TR_1 were a darlington instead of a transistor.

The op. amp. must have inputs compatible with ground in order to guarantee current limitation even in shortcircuit. With a negative voltage available, even of only a few volts, current limitation is simplified.

Fig. 36



LAYOUT CONSIDERATIONS

The performance of a regulator depends to a great extent on the case with which the printed circuit is produced. There must be no impulsive currents (like the one in the electrolytic filter capacitor at the input of the regulator) between the ground pin of the device (pin 3) and the negative output terminal because these would increase the output ripple. Care must also be taken when inserting the resistor connected between pin 4 and pin 3 of the device.

The track connecting pin 3 to a terminal of this resistor should be very short and must not be crossed by the load current (which, since it is generally variable, would give rise to a voltage drop on this stretch of track, altering the value of V_{ref} and threfore of V_o.

When the load is not in the immediate proximity of the regulator output "+ sense" and "– sense" terminals should be used (see fig. 37). By connecting the "+ sense" and "– sense" terminals directly at the charge terminals the voltage drop on the connection cable between supply and load are compensated. Fig. 37 shows how to connect supply and load using the sensing clamps terminals.

Fig. 37

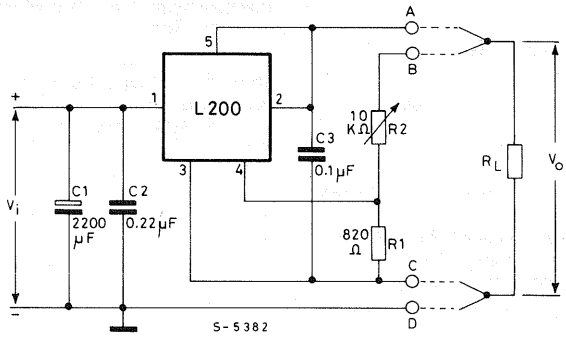
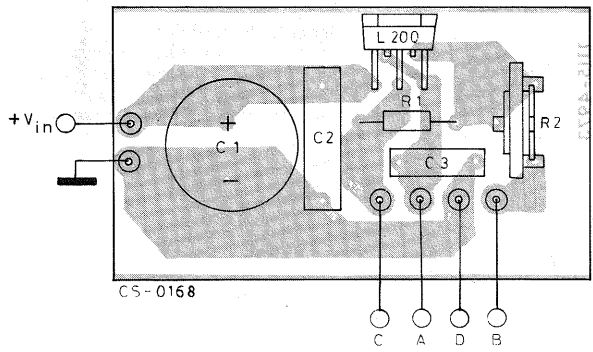


Fig. 38



HEATSINK DIMENSIONING

The heatsink dissipates the heat produced by the device to prevent the internal temperature from reaching values which could be dangerous for device operation and reliability.

Integrated circuits in plastic package must never exceed 150°C even in the worst conditions. This limit has been set because the encapsulating resin has problems of vitrification if subjected to temperatures of more than 150°C for long periods or of more than 170°C for short periods (24 h). In any case the temperature accelerates the ageing process and therefore influences the device life; an increase of 10°C can halve the device life. A well designed heatsink should keep the junction temperature between 90°C and 110°C. Fig. 39 shows the structure of a power device. As demonstrated in thermodynamics, a thermal circuit can be considered to be an electrical circuit where R1, 2 represent the thermal resistance of the single elements (expressed in °C/W);

Fig. 39

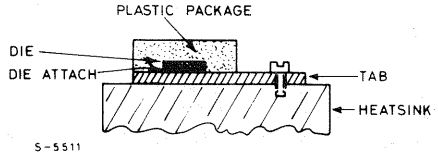
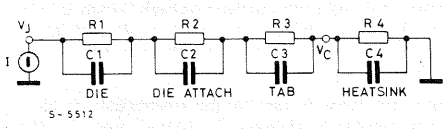


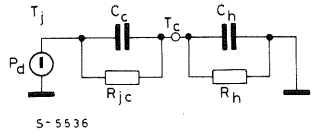
Fig. 40



C1, 2 the thermal capacitance (expressed in °C/W)
I the dissipated power
V the temperature difference with respect to the reference (ground).

This circuit can be simplified as follows:

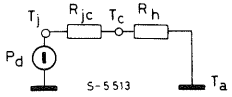
Fig. 41



Where C_e is the thermal capacitance of the die plus that of the tab.
C_h is the thermal capacitance of the heatsink
R_{jc} is the junction case thermal resistance
R_h is the heatsink thermal resistance.

But since the aim of this section is not that of studing the transistors, the circuit can be further reduced.

Fig. 42



If we now consider the ground potential as ambient temperature, we have:

$$T_j = T_a + (R_{jc} + R_h)\, P_D \qquad (1)$$

$$R_h = \frac{T_j - T_a - R_{jc} \cdot P_d}{P_d} \qquad (1a)$$

$$T_c = T_a + R_h \cdot P_d \qquad (2)$$

For example, consider an application of the L200 with the following characteristics:

$V_{in\ typ} = 20V$
$V_o = 14V$
$I_{o\ typ} = 1A$
$T_a = 40°C$
} typical conditions

$V_{in\ max} = 22V$
$V_o = 14V$
$I_{o\ max} = 1.2A$
$T_a = 60°C$
} overload conditions

$P_{d\ typ} = (V_{in} - V_o) \cdot I_o = (20-14) \cdot 1 = 6W$
$P_{d\ max} = (22-14) \cdot 1.2 = 9.6W$

Imposing $T_j = 90°C$ of (1a) we get (from L200 characteristics we get $R_{j-c} = 3°C/W$)

$$R_h = \frac{90 - 40 - 3 \cdot 6}{6} = 5.3°C/W$$

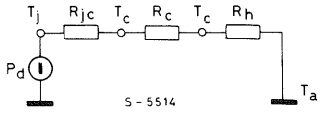
Using the value thus obtained in (1), we get that the junction temperature during the overload goes to the following value:

$$T_j = 60 + (3 + 5.3) \cdot 9.6 = 140°C$$

If the overload occurs only rarely and for short periods, dimensioning can be considered to be correct. Obviously during the shortcircuit, the dissipated power reaches must higher values (about 40W for the case considered) but in this case the thermal protection intervenes to maintain the temperature below the maximum values allowed.

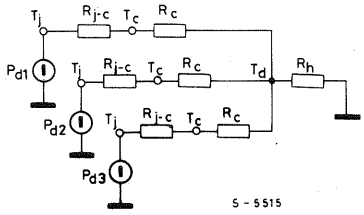
Note 1: If insulating materials are used between device and heatsink, the thermal contact resistance must be taken into account (0.5 to 1°C/W, depending on the type of insulant used) and the circuit in fig. 43 becomes:

Fig. 43



Note 2: In applications where one or more external transistors are used together with the L200, the dissipated power must be calculated for each component. The various junction temperatures can be calculated by solving the following circuit:

Fig. 44



This applies if the various dissipating elements are fairly near to one another with respect to the heatsink dimensions, otherwise the heatsink can no longer be considered as a concentrated constant and the calculation becomes difficult.

This concept is better explained by the graph in fig. 45 which shows the case (and therefore junction) temperature variation as a function of the distance between two dissipating elements with the same type of dissipator and the same dissipated power. The graph in fig. 45 refers to the specific case of two elements dissipating the same power, fixed on a rectangular aluminium plate with a ratio

of 3 between the two sides. The temperature jump will depend on the dissipated power and one the device geometry but we want to show that there exists an optimal position between the two devices:

$$d = \frac{1}{2} \cdot \text{side of the plate}$$

Fig. 46 shows the trend of the temperature as a function of the distance between two dissipating elements whose dissipated power is fairly different (ratio 1 to 4).

This graph may be useful in applications with the L200 + external transistor (in which the transistor generally dissipates more than the L200) where the temperature of the L200 has to be kept as low as possible and especially where the thermal protection of the L200 is to be used to limit the transistor temperature in the case of an overload or abnormal increase in the ambient temperature. In other words the distance between the two elements can be selected so that the power transistor reaches the $T_{j\ max}$ (200°C for a TO-3 transistor) when the L200 reaches the thermal protection intervention temperature.

Fig. 45

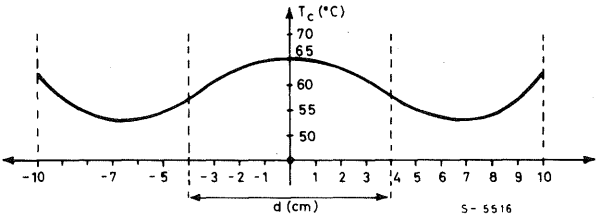
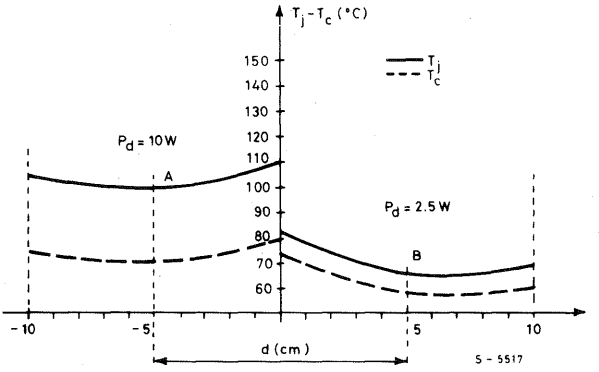


Fig. 46



A : Position of the device with high power dissipation (10W)
B : Position of the device with low power dissipation (2.5W)

TECHNOLOGY RELIABILITY AND APPLICATIONS OF SGS HIGH VOLTAGE NPN TRANSISTORS

by Pierandrea Borgato

Introduction

The basic technology chosen for high voltage (V_{CEO} > 400V - V_{CBO} > 600V) transistors is fundamental to their in-circuit performance as well as their "built-in" reliability.

Also the technology effects the wafer size which may be used in production, as well as the yields. In some cases also packaging options may be restricted. These are important factors influencing the price and availability for any semiconductor device.

Subject

This note discusses the SGS Multiepitaxial Mesa process used for a wide variety of industry standard products as well as some innovative types. (See pages 254, 255 and 256.

This technology is illustrated in simplified form in figure 1, figure 2 shows an actual cross section of the edge of a die made up of several scanning electon microscope pictures.

Fig. 1a - Multiepitaxial Mesa wafer simplified cross section

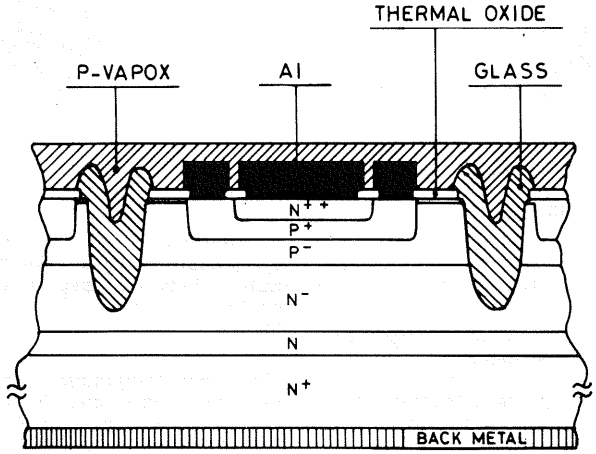


Fig. 1b - Multiepitaxial Mesa die in plan view

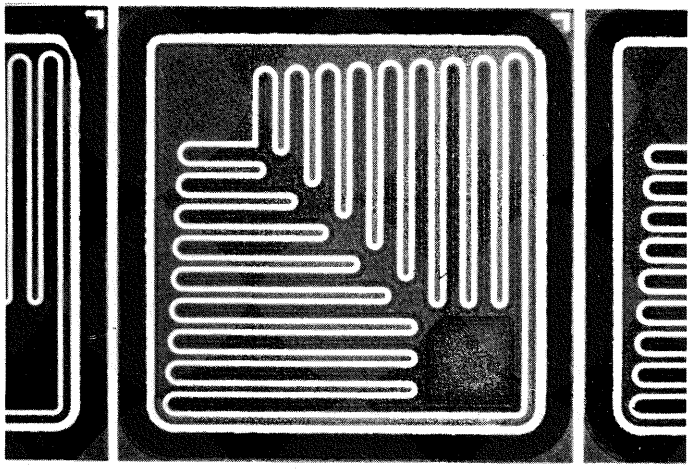
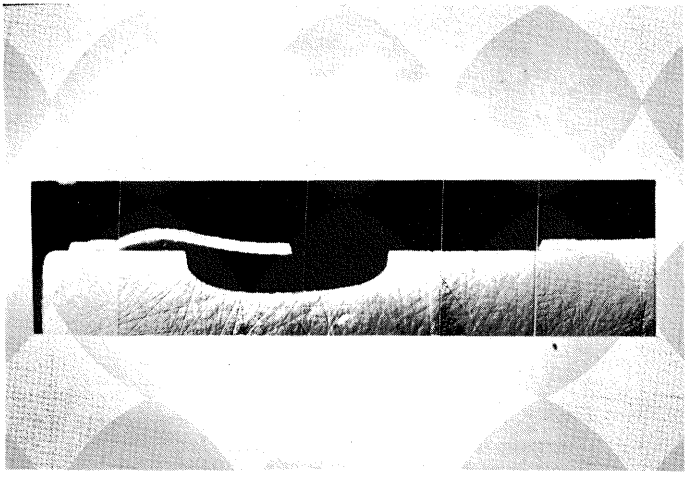


Fig. 2 - Actual section of Mesa edge termination



Features of the technology

Starting with an N^+ wafer, the N and N^- collectors layers are grown in specially developed epitaxial reactors, to produce the layered structure of the collector for the H.V. transistors.

The thicknesses required are much higher than used in integrated circuit technologies.

The intermediate N layer was interposed for the main purpose of achieving a very high $E_{s/b}$ and RBSOA capability.

An additional P^- layer is then grown, to increase the voltage breakdown. For this first critical phase SGS is fully equipped to grow epitaxial layers entirely "in house" while other power transistor manufacturers are mostly dependent on outside suppliers.

The P^+ base is produced by diffusion of boron into the final P^- layer and the N^+ emitter is diffused into the base. It is important to note that during this processing a relatively thick wafer is being

handled allowing SGS to use 4" and 5" wafers with ease.

Following diffusion is the etching of the mesa which is filled with a very pure glass by an SGS patented selective deposition process which avoids any contaminants such as photoresist which may not be entirely evaporated during the fusion of the glass. The aluminium top metal is now deposited and the pattern defined. The entire top of the wafer is now protected by a thick deposited oxide in which windows are opened for bonding the base and emitter connecting wires.

Finally the wafer is reduced to the correct thickness, removing the excess N^+ silicon by grinding the back of the wafer, after which the back is metallized.

Packaging

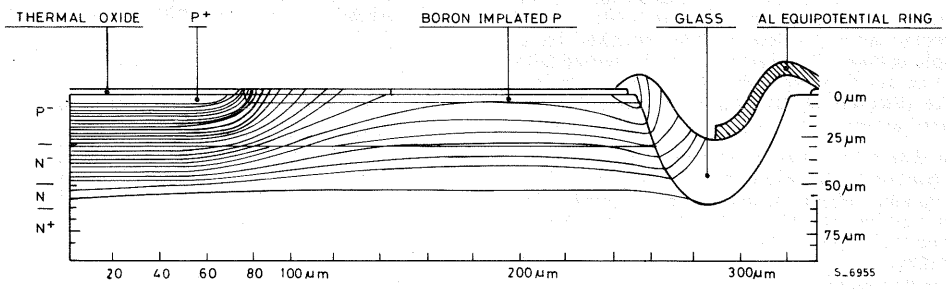
As the die must be separated from the wafer before mounting in the package the fact that SGS cuts the silicon outside the mesa and its glass filling, eliminates the risk of mechanical damage to the passivation.

As the sawing creates a short circuit at the edge of the die from the collector to the field plate no "flashover" can occur in the package between the header which is at collector potential and the top of the die, which in alternative half mesa technologies will be at base potential. The surface is covered with a thick oxide as previously mentioned so no arcing occurs along the surface.

This process of passivation also ensures high reliability in plastic packages.

This technology also allows wafers to be 100% probe tested to high voltage specifications, an important point for users of high voltage transistors in chip form for hybrid assemblies.

Fig. 3 - Section of Mesa with simulated equipotential lines



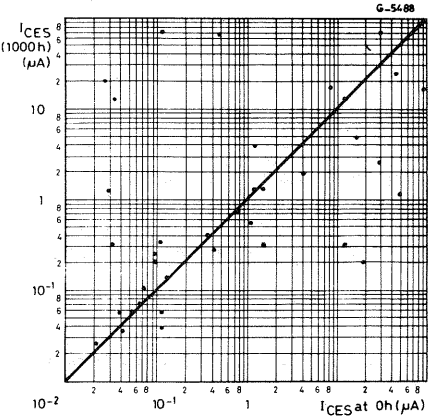
Reliability

In the reliability of a high voltage transistor the voltage stress on the surface of the silicon in the region of the collector/base interface is very important. This region must be protected from contamination. By terminating the collector-base junction on the edge of the mesa, and using glass the sealing against potential contaminants is assured. The use of the aluminium field plate ensures the glass is kept at a constant charge. The surface of the Player is treated with an ion implantation to ensure a very well controlled surface doping thus aiding close control of the electric field strenght distribution and leakage currents. SGS has developed computer simulation programs which can predict the field strength enabling the design to be optimised for reliability. Figure 3 shows the equipotential lines superimposed on the actual device cross section demostrating the low stress on the surface.

SGS continually monitors the reliability of the process by sampling production on a weekly basis. The high temperature reverse bias test (HTRB) is used to evaluate the stability and quality of the passivation.

Devices are subjected to T_{amb} = 125°C with the base-emitter shorted, and 600V d.c. is applied to the collector. Figure 4 shows typical results of leakage currents measured at V_{ces} = 900V, a point on the line at 45 degrees indicates no drift in

Fig. 4 - Leakage current stability in HTRB life tests



leakage. It is important to note that the currents involved are much lower than the specified maximum allowed by the data sheet. The devices with significant drift are those with initial leakage below 1μA and they remain below 80μA following 1000 hours of extreme stress.

Application hints

The basic rules of application for fast switching high voltage devices apply equally to SGS devices as well as other manufactures who use different technologies however some points deserve particular mention.

The multiple epitaxial structure with its "energy layer" provides an exceptional RBSOA, figure 5 shows the RBSOA of the BUX48/BUV48 which can sustain up' to 2A at 700V or 15A at 400V during the device turn-off with an inductive load.

Figure 6 shows the accidental overload safe operating area. The safe limit, up to 80A at any voltage up to 400V, is independent of the transistor base current, the lines with different base current indicate the maximum current which can be expected when the load is short circuited for any supply voltage. The overload must be sensed within 20 microseconds and the base drive removed at which time the accidental overload reverse bias safe operating area, swhown in figure 7, will apply.

This data shows that for occasional non-repetetive an overloads the multiepitaxial structure is exceptionally robust. As and indication devices have been stressed to 80A/400V for 40 microseconds during the on phase and then turned off at a P.R.F. of 100Hz for 4 hours without degradation - nearly 1.5 millon pulses!

Attention should be paid to correct turn-on base drive. The BUX48/BUV48 data shows the dynamic $V_{CE\ (sat)}$ characteristics (figure 8) which are significantly improved by ensuring an overshoot of I_{B1} illustrated in figure 9.

Fig. 6 - Accidental overload SOA of BUX48/BUV48

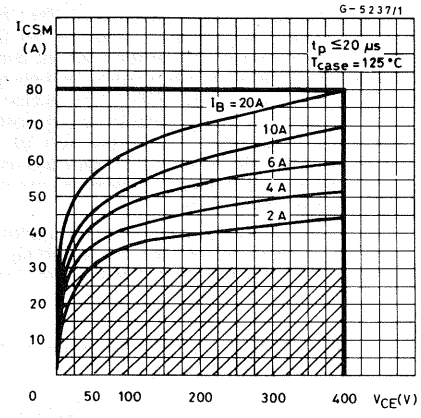


Fig. 7 - Accidental overload RBSOA of BUX48/BUV48

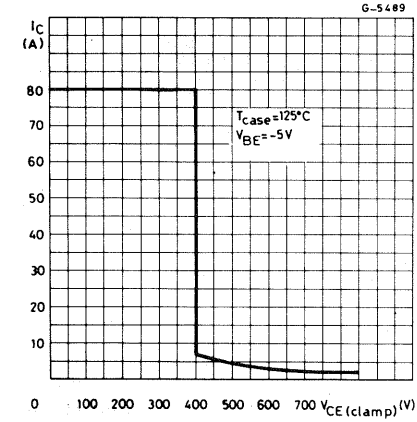


Fig. 5 - RBSOA of SGS BUX48/BUX48A (TO-3), BUV48/BUV48A (SOT-93)

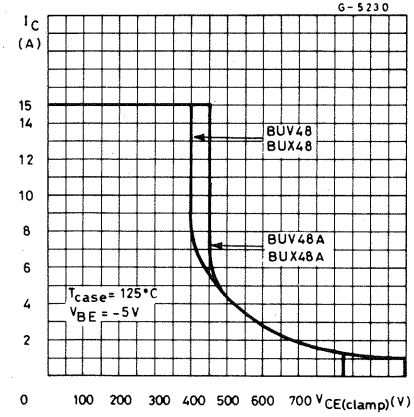


Fig. 8 - Dynamic $V_{CE\ (sat)}$ of BUX48/BUV48

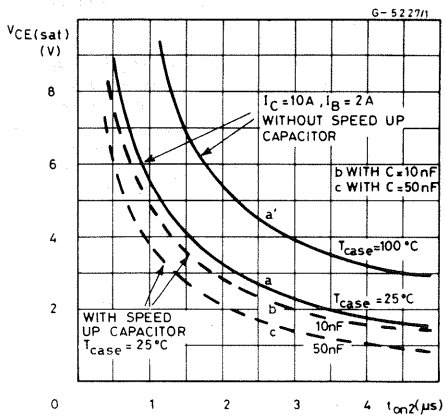
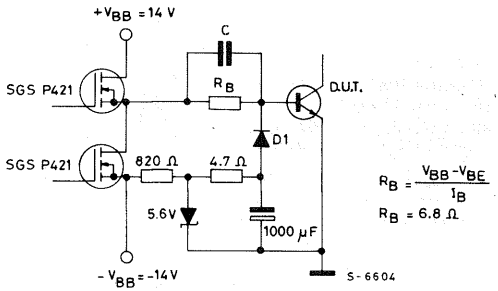


Fig. 9 - I_{B1} waveform for improved dynamic saturation

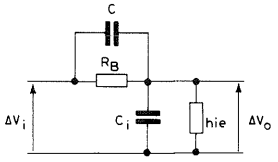
$V_{CE\ (sat)}$ dynamic test circuit



$$R_B = \frac{V_{BB} - V_{BE}}{I_B}$$

$R_B = 6.8\ \Omega$

Equivalent input schematic circuit at turn-on

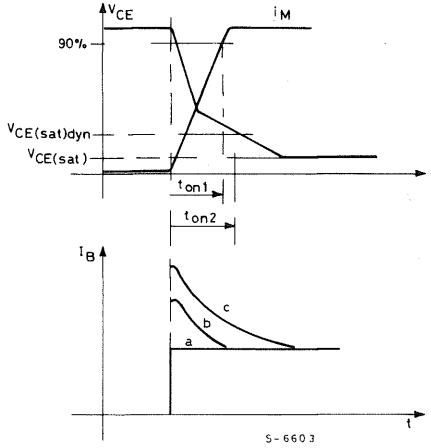


$$\Delta V_o = \Delta V_i \frac{C}{C_i + C}$$

if $C \gg C_i$ $\Delta V_o = \Delta V_i$

S-6605/1

Remarks to $V_{CE\ (sat)}$ dyn. test circuit



The speed-up capacitor decreases the $V_{CE\ (sat)}$ dyn. as shown in the diagram and modifies the shape of the base current with an overshoot.

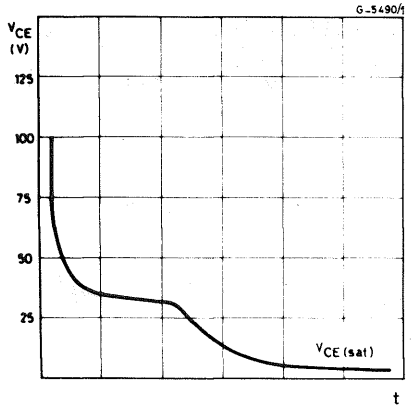
A slow rise time of I_{B1} can result in extremely high turn-on losses, as shown in figure 10 the multi-epitaxial device will have a V_{CE} of around 40V for some microseconds. This results in higher junction temperatures and in turn longer turn-off switching times, sometimes these longer turn-off times are misinterpreted as being a "cause" rather than an "effect". This can be cured by similar solutions as used to improve dynamic $V_{CE\,(sat)}$.

Conclusion

The Multiepitaxial Mesa process has been demonstrated to be a high volume, cost effective process yielding products with high intrinsic reliability and exceptional ruggedness to enhance field reliability.

The process is very flexible being readily "pilotable" to produce higher voltage or higher current "sub families" with good yield, thus avoiding the risks for both the user and the suppliers of selections from lower performance types.

Fig. 10 - High turn-on loss caused by too slow I_{B1} rise time



SGS FASTSWITCH™ HOLLOW EMITTER TECHNOLOGY

- HIGH VOLTAGE
- VERY FAST SWITCHING
- HIGH EFFICIENCY
- IMPROVED RELIABILITY
- HIGH POWER

INTRODUCTION

Hollow emitter technology fills the gap in power transistor technology between bipolar and power mos by providing an economic solution to high voltage switching.

This new technology is ideally suited to switching frequencies which cause problems to both bipolar and power mos devices. The SGS FASTSWITCH™ range has been developed for rugged operation at very high switching speeds, its high efficiency allows more compact designs with smaller heatsinks.

Hollow emitter technology has been designed to improve the performance of SGS Multiepitaxial Mesa power transistors. When compared to industry standard high voltage devices, hollow emitter types provide faster switching times and a lower saturation voltage. The term "hollow emitter" refers to the missing centre region in the emitter area, this hollow emitter reduces the charge crowding effect in the centre of the emitter and thus reduces the storage time to remove the excess charge. Hollow emitter devices also benefit from a thinner intermediate N layer which reduces the collector resistivity and the saturation voltage.

SUBJECT

This note covers the current range of FASTSWITCH™ devices which are rated up to 12A I_C (continuous), up to 1000V V_{CES} and up to 450V V_{CEO}. Inductive fall time is as low as 0.08μs at 100°C. The current range of devices is shown in table 1.

The technology is illustrated in simplified form in figure 1, this drawing shows the hollow emitter section with a reduced intermediate N layer when compared to the standard Multiepitaxial Mesa illustration, Fig. 1b.

Table 1 - SGS "Hollow Emitter" FASTSWITCH™ products

I_C (A)	V_{CBO} (V)	V_{CEO} (V)	P_{tot} (W)	Package	TYPE	@ h_{FE} (min)	@ I_C (A)	@ V_{CE} (V)	V_{CEsat} max (V)	@ I_C (A)	@ I_B (mA)
5	700	400	90	TO-220	**SGSD00042**	4	4	1	1	4	1000
5	1000	450	90	TO-220	**SGSD00044**	4	3.2	1	1	3.2	800
8	700	400	90	TO-220	**SGSD00040**	5	6	1.5	1.5	6	1200
8	700	400	120	SOT-93	**SGSD00037**	5	6	1.5	1.5	6	1200
8	700	400	120	TO-3	**SGSD00036**	5	6	1.5	1.5	6	1200
8	1000	450	90	TO-220	**SGSD00041**	5	6	1.5	1.5	6	1200
8	1000	450	120	SOT-93	**SGSD00039**	5	6	1.5	1.5	6	1200
8	1000	450	120	TO-3	**SGSD00038**	5	6	1.5	1.5	6	1200
12	700	400	150	SOT-93	**SGSD00033**	5	10	1.5	1.5	10	2000
12	700	400	175	TO-3	**SGSD00032**	5	10	1.5	1.5	10	2000
12	1000	450	150	SOT-93	**SGSD00035**	5	8	1.5	1.5	8	1600
12	1000	450	175	TO-3	**SGSD00034**	5	8	1.5	1.5	8	1600

Fig. 1a - Structure of the hollow emitter technology

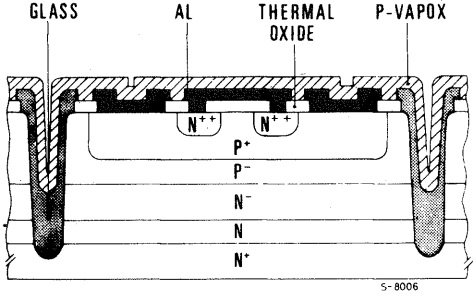
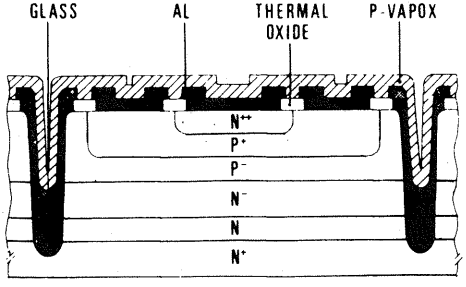


Fig. 1b - Structure of the standard Multiepitaxial Mesa technology



COMPARISON BETWEEN STANDARD & THE NEW HOLLOW EMITTER TECHNOLOGY

Hollow emitter technology is a development of the standard high voltage multiepitaxial mesa technology. In this new technology the emitter is not diffused over the normal area. In fact only on the normal emitter edge.

The purpose of this difference is to overcome the charge-crowding effect in the centre of the emitter during the off transition found in industry standard high voltage devices and hence achieve much faster switching times.

STANDARD HIGH VOLTAGE

Analysing the charge in normal high voltage devices shows that during the ON transition the charge is easily built up on the edge of the emitter but the increase in base resistance towards the centre of the emitter reduces the charge level at the centre.

During the OFF transition the base extraction current can rapidly eliminate the charge at the edge of the emitter, but the charge at the centre is removed with some difficulty owing to the transversly distributed resistance in the base under the emitter finger.

When the edge is already turned off, a level of charge remains at the centre of the emitter diffusion which slows down the turn-off time.

Fig. 2a and 2b illustrates both conditions.

HOLLOW EMITTER

In FASTSWITCH™ transistors, diffusion at the centre of the emitter is prevented by appropriate

Fig. 2a - Charge condition during conduction - Normal high voltage technology

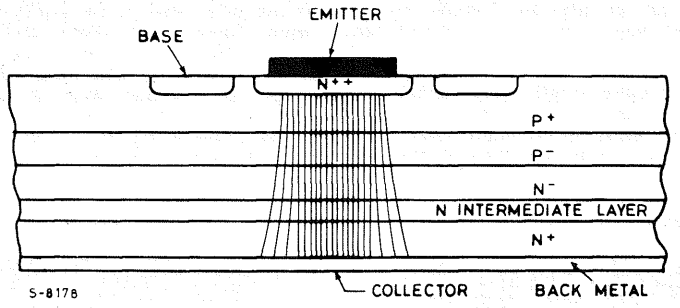


Fig. 2b - Charge remaining after turn-off

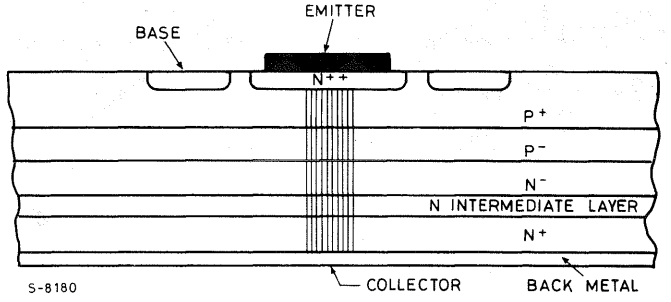
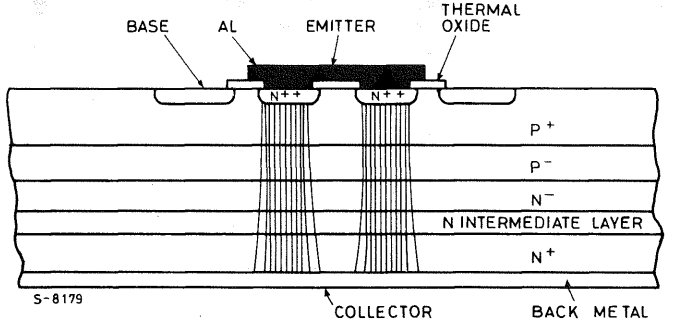


Fig. 2c - Charge condition during conduction - Hollow emitter technology



masking, and the resulting hollow in the emitter prevents the accumulation of the charges which would slow down the turn-off time.

Fig. 2c illustrates the charge condition for hollow emitter diffusion.

Removing the centre region and therefore reducing the emitter area has a negligible effect on V_{CEsat} for two reasons - firstly, the centre region of the standard device carries less charge, and secondly, the intermediate N layer is thinner which reduces the collector resistivity.

The result is a device with extremely fast switching times and improved efficiency.

COMPARISON OF SWITCHING TIMES

By comparing a standard Multiepitaxial Mesa device (BUX48) with a hollow emitter device (SGSD00032) of the same dimensions and similar static characteristics, the hollow emitter device shows a clear improvement in fall time and a small improvement in storage time. With reference to the switching characteristic curves (Fig. 3a) it can be seen that with resistive loads, this improvement exists over a wide variation of collector current.

The benefit of reduced fall and storage times automatically achieves a reduction in dissipated

energy in the device during turn-off. Energy dissipation for both technologies is compared in Fig. 3b and it can be seen that hollow emitter technology again shows a significant improvement over Multiepitaxial Mesa.

Hollow emitter devices benefit from the same improvements in storage and fall times and hence energy dissipation when loaded inductively. Table 2 lists a selection of devices and shows typical comparitive switching times between FASTSWITCH™ and Multiepitaxial Mesa devices when tested with an inductive load. It can easily be seen from the results that each FASTSWITCH™ device shows a marked improvement in switching time for both base and emitter switching. A further useful feature is that both base and emitter switching times are almost always equally low with hollow emitter devices e.g. SGSD00035 t_{fall} is 50ns for both switching conditions.

Fig. 3a - Storage and fall times

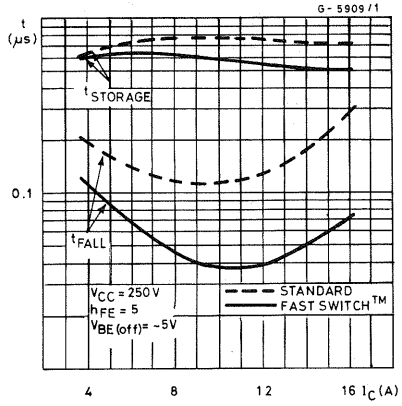


Fig. 3b - Dissipated energy

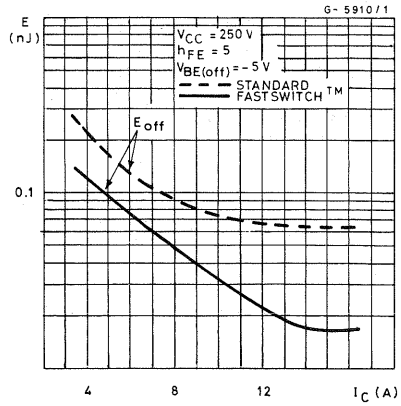


Table 2 - Typical tf and ts with an inductive load

DEVICE	IC(A)	EMITTER SWITCHING		BASE SWITCHING		TECHNOLOGY
		tstorage	tfall	tstorage	tfall	
BUX48	10	500ns	100ns	2μs	200ns	MULTIEPITAXIAL MESA
BU508A	5	800ns	300ns	6μs	400ns	MULTIEPITAXIAL MESA
SGSD00031	10	400ns	100ns	1.2μs	100ns	PALNAR DARLINGTON
BU810	5	300ns	150ns	800ns	150ns	PLANAR DARLINGTON
SGSD00035	10	300ns	50ns	800ns	50ns	FASTSWITCH™
SGSD00039	5	300ns	40ns	700ns	50ns	FASTSWITCH™

REVERSE BIAS SAFE OPERATING AREA (RBSOA)

The reduction in thickness of the intermediate N layer plus increased switching speed with hollow emitter devices result in RBSOA characteristic changes. Fig. 4a shows two comparable devices, one from each technology. It can be seen from the RBSOA characteristic curves that although the BUX48 has a better RBSOA at 400V, the SGS hollow emitter device has been optimised to give an improved RBSOA at higher voltages to suit switch mode power supply applications. A typical load line for a hollow emitter device in a switch mode power supply with snubbing is shown in Fig. 4b. It can be seen that the hollow emitter device provides more protection at the higher voltages which is evenly balanced with adequate protection in the lower voltage and high current area.

Fig. 4a - Reverse bias safe operating area

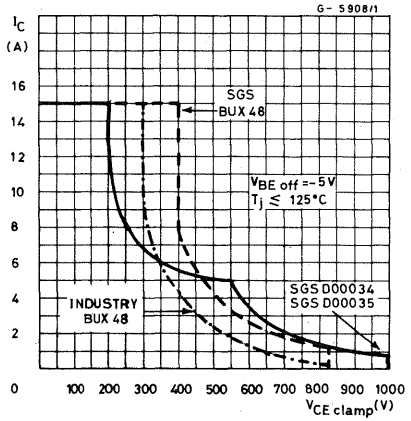
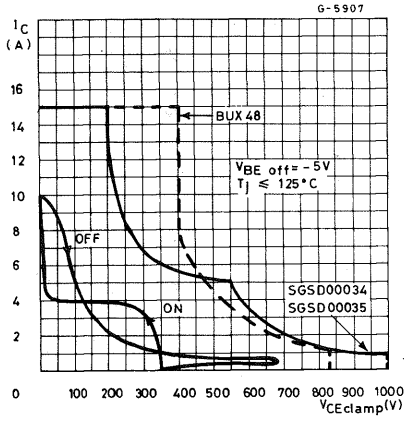


Fig. 4b - Reverse bias safe operating area with typical load line for SMPS application



APPLICATIONS

The FASTSWITCH™ technology has been specifically optimised to produce devices with extremely short switching times with respect to their high voltage and current capability. The resulting high efficiency of these devices make them ideally suited for today's electronic solutions to energy saving where fast switching is of prime importance.

For these reasons, hollow emitter transistors have properties which are ideally suited to:

- INVERTERS
- SWITCHING REGULATORS
- FLUORESCENT LIGHTING
- DEFLECTION CIRCUITS (high definition display)

CONCLUSIONS

Hollow emitter FASTSWITCH™ devices provide an economic solution to high voltage switching in the frequency range 20-70KHz. High efficiency and very fast switching result in smaller heatsinks, lower cost and improved reliability.

There are suitable types in the SGS FASTSWITCH™ series to replace most common high voltage industrial power transistors so the majority of users can benefit from the significant advantages of this new technology.

PARALLELING HIGH-VOLTAGE TRANSISTORS FOR HIGH CURRENT SWITCHING

The requirement for higher and higher powers from convertor and invertor circuits leads to the necessity of high-voltage devices with ever increasing current ratings.

These requirements would necessarily lead to the use of extremely large area die. For example a transistor with $V_{CEO} > 400V$ and $V_{CE(sat)}$ at $20A/4A < 1.5V$ would require a die with an area greater than $90Kmils^2$ ($>$ 300mils x 300mils) [$>$ 7.5mm x 7.5mm]. Such a product would be very expensive and have lower reliability, due to the difficulty of making a die attach which will withstand power cycling without reverting to expensive molybdenum bases. A different possibility for obtaining higher output currents is to use more than one high-voltage device connected in parallel. In the following note this solution is analysed, with special reference to the problem of current sharing in the paralleled transistors both in saturation and in switching conditions.

EQUALIZATION OF COLLECTOR CURRENT DURING SATURATION

The most important electrical parameter in the saturated operation of parallel connected power devices is $V_{CE(sat)}$. The imperfect splitting of the current in the different parallel branches is substantially a consequence of the different $V_{CE(sat)}$'s of the used transistors. Variation of $V_{BE(on)}$, and $V_{BE(sat)}$ may also be a factor but is not so significant, as, if one device carried a higher current its $V_{BE(sat)}$ will tend to increase so diverting more base current to the other device. When we consider two transistors with base current high enough to keep them in the saturated area (Fig. 1), the saturation voltage for each device is expressed by:

$$V_{CE(sat)} = I_C \times r_{CE(sat)}$$

Fig. 1

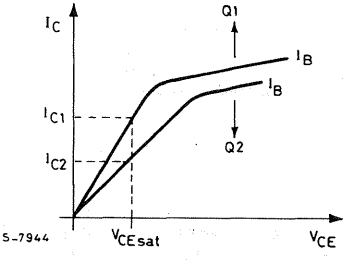
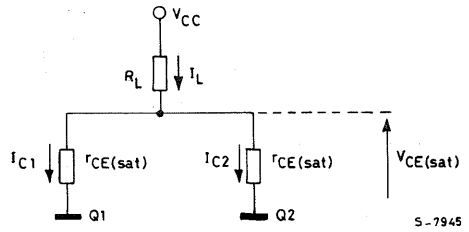


Fig. 2



When two transistor have to carry an overall current, I_L, from the equivalent circuit shown in Fig. 2, I_{C1} and I_{C2} may be calculated. In fact, it follows that:

$$I_{C1} = \frac{V_{CE(sat)}}{r_{CE(sat)\,1}}$$

$$I_{C2} = \frac{V_{CE(sat)}}{r_{CE(sat)\,2}}$$

where $V_{CE(sat)} = I_L \times \frac{r_{CE(sat)\,1} \times r_{CE(sat)\,2}}{r_{CE(sat)\,1} + r_{CE(sat)\,2}}$

A possible equalization may be achieved by connecting, to the emitters of the transistors, resistances whose value is high enough when compared to the saturation resistance $r_{CE(sat)}$; in this way, the equalization of collector currents is improved by a factor $r_E/r_{CE(sat)}$.

An evident limitation for this kind of equalization is the power dissipated in the emitter resistances. For each transistor, in fact the following is true.

$$P_{rE} = \$ I_E^2 \times rE$$

where \$ is the duty cycle.

When N transistors are connected in parallel, N x P_{rE} has to be significantly low when compared to the useful power, so that the overall efficiency isn't decreased too much.

In the experimental work the high voltage devices BUX48 and BUV48 have been considered, the evalutation circuit is shown in Fig. 3.

Fig. 3

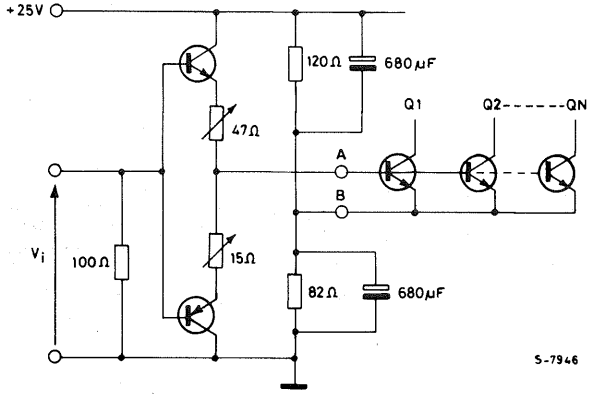


Figure 4b shows the behaviour of the collector currents with emitter resistors and Figure 4a without emitter resistors. Q1 has $V_{CE(sat)}$ 0.4V at 10A/2A and Q2 $V_{CE(sat)}$ 1.5V at 10A/2A. Figure 5 shows the published data for BUX48, when the V_{BE} is equal the spread of I_C can be estimated.

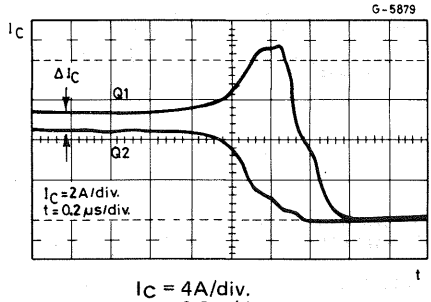
Measuring conditions are shown in Fig. 6. From figures 4a and 4b it may be verified that the delta I_C of 3.2A in the unequalized condition is reduced to negligible values when two emitter resistances of 0.25Ω are used.

The dissipated power, calculated for \$ = 0.5, is:

$$Pd = 2 \times \$rE \times I_{E2} = 2 \times 0.5 \times .25 \times 10^2 = 25W$$

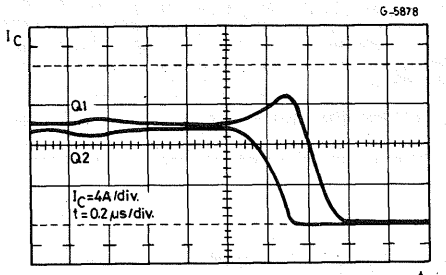
The mentioned example can therefore be considered as a limit condition, as the used samples of BUX48 show $V_{CE(sat)}$ similar to the lowest likely limit and the maximum guaranteed value.

Fig. 4a -Without emitter resistor



I_C = 4A/div.
t = 0.2µs/div.

Fig. 4b - With emitter resistors



I_C = 4A/div
t = 0.2μs/div.

Fig. 5

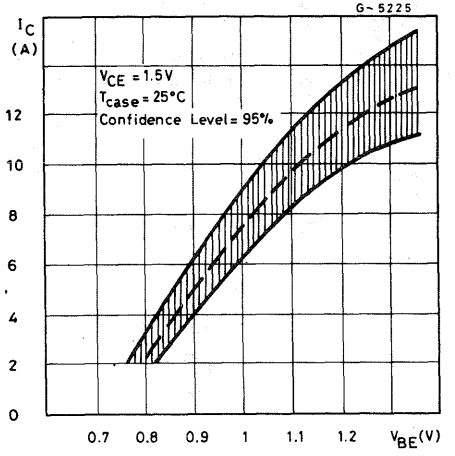
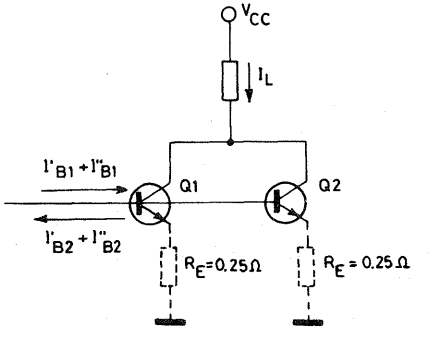


Fig. 6



V_{CC} = 300V
I_L = 20A
$I'_{B1} + I''_{B1}$ = 4A
$I'_{B2} + I''_{B2}$ = -8A

As a general rule, we have seen that a voltage on the sharing resistors of the same order of magnitude as V_{BE} (1 - 1.5V) is sufficient to obtain good equalization in the saturation condition for all the devices. In this case the total $V_{CE(on)}$ becomes similar to the $V_{CE(sat)}$ of a high voltage darlington which has a much better current capability for a given silicon area. The use of a darlington could, in some cases, avoid the need to parallel transistors. For example one SGSD310 offers twice the $I_{C(sat)}$ of a BUX48 for a smaller silicon area.

The experimental tests have been performed using 2 or 3 samples connected in parallel and considering in each case 1 or 2 transistors respectively at the upper $V_{CE(sat)}$ limit.

The measuring conditions considered for BUX48 are:

V_{dc} = 300V
I_C = 10A for each branch of the parallel connection
I_{B1} = 2A
I_{B2} = -2A

EQUALIZATION OF COLLECTOR CURRENT DURING SWITCHING

An item of fundamental importance in the parallel connection of high voltage transistors is that related to the proper operation of devices during switching.

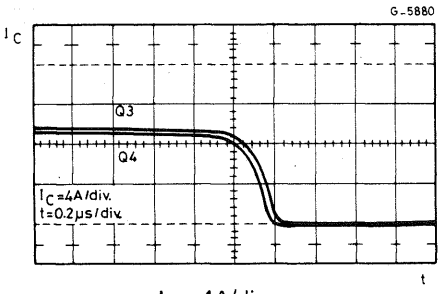
As far as the turn-on is concerned, the problem doesn't really exist; the faster transistors would tend to carry all the load current, but the consequent exist from saturation would determine a limitation of the current flowing through them. This special negative feedback effect allows during turn-on a good sharing of the current in the parallel branches.

During turn-off, on the contrary, the currents in the individual transistors can't be controlled anymore; the devices featuring a longer storage time have to carry, after the turn-off of the faster transistors, all the current forced by the load.

During the turn-off phase, high-voltage transistors are normally subject to special base conditions (high reverse base current required for fast switching) which limits the maximum energy that the devices can dissipate during this time ($E_{s/b}$). It is clear that the slower transistors, having to switch high current peaks, are subjected, during this operating phase, to especially heavy voltage - current combinations, and consequent dangers of operation outside the safe RBSOA limits.

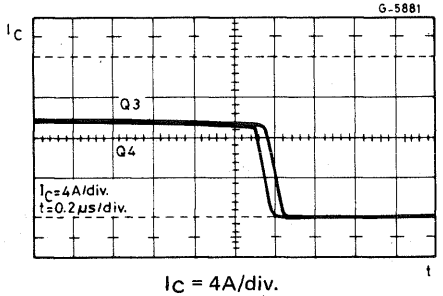
The electrical parameters that more directly influence the turn-off (t storage and t fall) in high-voltage devices are $V_{CE(sat)}$ at working collector and base currents, and h_{FE} in the active area (closer to the current at which the peak gain occurs). The transistors used in the experimental work have therefore been selected not only for $V_{CE(sat)}$ (as seen in Section 1), but also for h_{FE}.

Fig. 7a - Resistive Load



Ic = 4A/div.
t = 0.2μs/div.

Fig. 7b - Inductive load



Ic = 4A/div.
t = 0.2μs/div.

Figures 7a and 7b show the behaviour of the collector currents at turn-off for two BUX48 transistors, both with a resistive load and with an inductive load (with "clamp"). The measuring conditions and the measured electrical parameters for both transistors are:

Measuring conditions	**Parameter measurements**
V_{dc} = 300V	h_{FE} (4A, 5V) = 20.4
I_C = 10A for each of the parallel branches	$V_{CE(sat)}$ (10A, 2A) = 0.6V
I_{B1} = 2A	h_{FE} = (4A, 5V) = 20
I_{B2} = 2A	$V_{CE(sat)}$ (10A, 2A) = 0.5V

From the current behaviour it is possible to verify that because the transistors have been selected showing the same $V_{CE(sat)}$ and the same h_{FE} a perfect equalization is obtained during switching with either resistive or inductive load, without any special precautions.

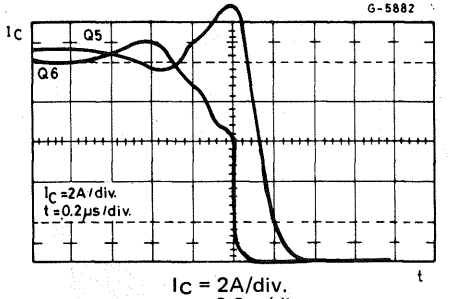
On the other hand, Fig. 8 shows the turn-off currents for two BUX48 transistors, different both in gain and in $V_{CE(sat)}$.

These waveforms have been obtained by equalizing the collector currents with emitter resistors but without any special precautions during the switching phase.

The transistor (Q5), featuring an $h_{FE} > 80$ (at I_C = 1A, V_{CE} = 5V) and a $V_{CE(sat)}$ of 0.4V (at I_C = 10A, I_B = 2A) is significantly slower in "t storage" when compared to transistor (Q6), featuring, in the same conditions, an h_{FE} of 20 and $V_{CE(sat)}$ of 1.4V.

It is clear that the slower transistor (Q5) has to switch a high current peak and is, as previously mentioned, more heavily stressed during this phase.

Fig. 8



Ic = 2A/div.
t = 0.2μs/div

Fig. 9a

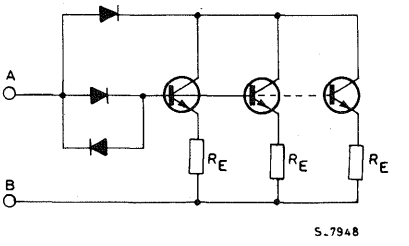
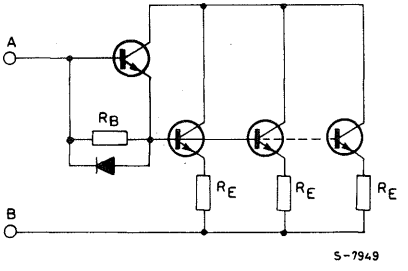


Fig. 9b



Two possible circuit precautions enabling a good sharing of current both in saturation and in switching conditions are shown in Fig. 9. These obtain equalization of storage times even if the transistors have very different saturation and gain characteristics.

An improvement of collector current equalization at switching is obtained by limiting the spread of storage times of the transistors. The easiest way to

achieve this is to minimise the storage time so that the differences become negligible. When a transistor is prevented from going into hard saturation, i.e. with base collector junction not forward biased, the storage time is inherently very low.

Fig. 10 is related to the switching of transistors Q5 and Q6, obtained with the circuit shown in Fig. 9a.

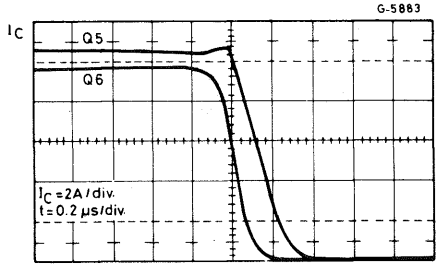
For the case of three parallel connected transistors, the devices have been selected so that two of them show a low gain and a high $V_{CE(sat)}$, therefore being much faster than the third one, the latter being featured by a very high gain and a low $V_{CE(sat)}$. It is clear that this is the worst case, as the latter transistor has to switch practically all the load current.

Fig. 11 shows the behaviour of the collector currents, in the case of an inductive load, for three BUX48 transistors, selected according to the previous criteria.

Measured parameters

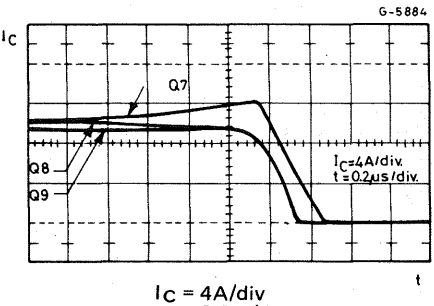
h_{FE7} (1A, 5V) = 50
$V_{CE(sat)7}$ (10A, 2A) = 0.45V
h_{FE8} (1A, 5V) = 20
$V_{CE(sat)8}$ (10A, 2A) = 1.4V
h_{FE9} (1A, 5V) = 20
$V_{CE(sat)9}$ (10A, 2A) = 1.4V

Fig. 10



Ic = 2A/div
t = 0.2µs/div.

Fig. 11



Ic = 4A/div
t = 0.2µs/div.

CONCLUSION

The gain characteristics influence the bahaviour of the parallel connected transistors both during saturation and switching phases. The tests performed on BUX48 devices show that through simple circuit precautions and limited power dissipations it is possible to obtain good current sharing during the different working phases.

To achieve high current devices manufacturers parallel transistor die within one package. For example the BUX98 is two BUX48 die mounted in a TO-3 package and an SGS40TA045 is four BUX48 die assembled in the TO-240 high power module. No particular precautions are required as the die used are neighbours from one wafer, consequently all their parameters are inherently very well matched. Thus the designer may treat these multi-chip devices as a single transistor in any circuit conditions.

With a suitable safety margin in design the need for emitter ballast resistors is removed. To achieve good sharing during turn-off the devices must be kept out of over saturation, the darlington connection of a driver transistor achieves this with the bonus of increased forward gain. This demonstrates the logic of using high voltage darlingtons in place of transistors and that in the case when even higher currents are required the paralleling of darlingtons will be less critical than transistors.

SECOND BREAKDOWN IN POWER TRANSISTORS

One of the basic failure machanisms in power transistors is second breakdown.

Under this term, various physical phenomena which are completely different are included. They depend on the different use of transistors in the circuits and have in common the electrical and thermal instability inherent in transistors themselves.

The conduction behaviour of an emitter base junction and the current gain of a transistor depend significantly on the temperature and increase as a function of the temperature. Electrical and thermal instabilities may simultaneously act within the device, thereby giving rise to destructive second breakdown mechanism.

An understanding of this mechanism is of great importance for a safer and optimum application of a power transistor.

A distinction should be made between direct second breakdown ($I_{s/b}$ or more commonly SOA), which is distinguished by a normal direction of base current I_B (entering in an NPN transistor) and inverse second breakdown ($E_{s/b}$), when I_B is in the opposite direction (extracted from an NPN transistor). The limits to which a transistor may be used without entering into $E_{s/b}$ are defined by the reverse bias safe operating area (RBSOA).

DIRECT SECOND BREAKDOWN ($I_{s/b}$)

An important information for the power circuit designer is the locus of I_C - V_{CE} points defining the boundary between stable and unstable operation of forward biased transistors. This locus defines the SOA (safe operating area) that is the area of the $\log I_C$ - $\log V_{CE}$ plane which may be used without any risk in DC current conditions or with different width pulses at a known temperature. A typical SOA is shown in Fig. 1.

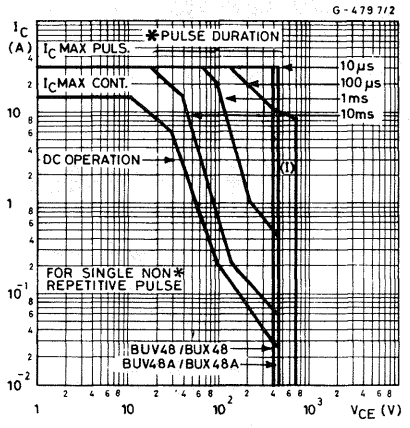
The limits of this area are the following:

1) The A-B section represents the upper limit of the collector current that may normally be used, generally limited by wire bonds. Operation at higher currents may cause damage to the wires of their bonding.

2) The B-C section is the -1 slope curve section (i.e. the section with constant dissipation) defined by:

$$V_{CE} \times I_C = P_{max} = \frac{(T_{j\,max} - T_o)}{R_{th}}$$

Fig. 1 - Safe operating areas



This section therefore indicates the maximum dissipable power of the device. T_{jmax} is the maximum temperature which the collector-base junction may reach, over which the device reliability may be compromised. In power transistors, T_{jmax} varies between 125 and 200 degrees C and generally depends on the metallurgy and the type of package.

R_{th} is the thermal resistance between the collector-base junction and the case, including all the silicon and package system. It may be observed that the increase of the maximum dissipable power when the pulse width decreases (Fig. 1) corresponds to the decrease of Z_{th} with respect to R_{th}.

3) The section C-D corresponds to the second breakdown phenomenon (or $I_{s/b}$) and limits the maximum power that the transistor can dissipate. This may occur even at relatively low V_{CE} voltages.

4) The section D-F is the limit due to the transistor's BV_{CEO}.

Second breakdown is generated by the electrical and thermal instability of the transistor. The main causes of this instability are;

1) The V_{BE} of a directly biased base-emitter junction, at constant current, decreases linearly with temperature, with a ϕ = 2 to 2.5mV/°C slope. The base current of the transistor may therefore be expressed by:

$$I_B = I_o \times e^{q\frac{(V_{BE}-\phi T)}{KT}}$$

and, when V_{BE} is kept constant, it increases with temperature.

2) The h_{FE} at the relevent voltage values increases as a function of temperature according to the law:

$$h_{FE} = h_{FEo} \times e^{(\Delta Eg/KT)}$$

where ΔEg is an activation energy which is a feature of the transistor.

3) The thermal conductivity of silicon decreases when temperature is increased, therefore worsening the thermal resistance of the transistor.

When these three phenomena are taken into consideration, it may be seen that a pulse of power $P = V_{CE} \times I_C$ generates:

a) an increase of the junction temperature, giving rise to an increase of I_B and h_{FE}, threfore to an increase of I_C, with a following increase of P and, therefore, a further temperature increase.

b) a dissipation to the external environment, controlled by the thermal resistance $R_{th} = dT/dP$ which tends to stabilize the device.

The situation evolves towards stability when:

$\frac{\Delta I_{C2}}{\Delta I_{C1}} = \frac{\partial I_C}{\partial T} \times V_{CE} \times R_{th}$ is smaller than 1, or instability if > 1.

In this way, a stability factor may be defined that will be a function of V_{CE} and I_C:

$$S = R_{th} \times V_{CE} \times \frac{\partial I_C}{\partial T}$$

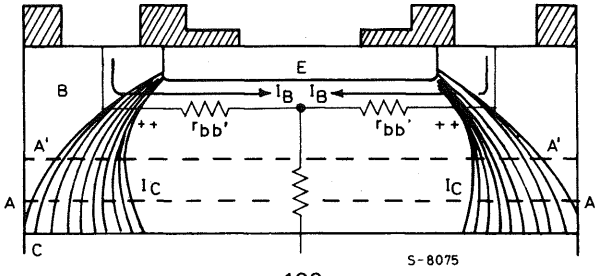
When S > 1 so called "thermal runway" occurs and the junction temperature increases without any limit, therefore degrading and possibly damaging the transistor. The failure generally occurs when the surface temperature becomes greater than the eutectic temperature between silicon and the contact metal (front aluminium) with a consequent melting of the alloy.

Also, it may happen that a localized temperature increase damages the crystal. or that the inner temperature of the device reaches values high enough to melt the silicon.

For the understanding of $I_{s/b}$ phenomena giving rise to a reduction of the maximum power that the transistor can dissipate as V_{CE} increases (zone D - E) it is necessary to take into account that device operation isn't homogeneous on all the dice area. There are disuniformities in the emitter base current density, that may be due to junction disuniformities, crystal defects and, most of all. to the emitter edge concentration phenomenon.

The voltage drop due to the base current flowing through the cross resistance rbb' gives rise to a disuniformity of V_{BE} at the junction, therefore to the disuniformity of the current density J_E (see Fig. 2).

Fig. 2



A side drop of 26mV reduces by a 1/e factor the injected emitter current.

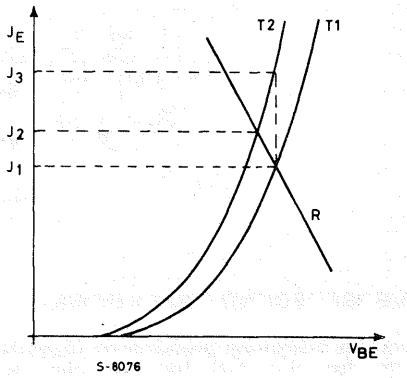
A concentration is therefore generated of the current at the emitter periphery, therefore the active silicon area is reduced and hot spots occur, leading to an effective increase of the thermal resistance. As a result, the maximum dissipable power is decreased.

When V_{CE} is increased the effect of the base - collector electric field is to increase the base current concentration.

Different techniques may be adopted to limit the $I_{s/b}$ phenomenon. Fundamentally, they consist of minimising the mechanisms that trigger electrical and thermal instabilities in the transistor. The basic techniques are:

1) Minimization of crystal damages, metal impurities and of doping disuniformities.
2) Optimization of package and die attach techniques, to minimize the thermal resistance on which the stability factor S depends. Disuniformities of silicon die bondings to the case may give rise to adverse variations of R_{th} as a macroscopic parameter for the dice as a whole, but also to significant variations between different points, giving rise to premature second breakdown.
3) Increase of the base thickness to reduce the high current densities (due to emitter crowding) flowing through the collector base junction (where the electric field is localized), so that the density of the dissipated power is decreased. High base thicknesses, however, will result in lower cut off frequencies and slower switching times.
4) Optimization of the horizontal geometry.
5) Introduction of distributed ballast resistances connected in series with the base, the emitter or both, which tend to give a negative feedback to thermal runaway, therefore stabilizing the device. Fig. 3 shows the J_E/V_{BE} characteristic curves for two points in the junction, at different temperatures (T2 > T1).

Fig. 3



It may be seen that the introduction of a ballast resistance in series with the base or the emitter may reduce from J_3 to J_2 the current density in the hot spot.

The emitter ballast resistance is generally obtained by opening emitter contacts thinner than the emitter strip (Fig. 4).

In this way it is possible to limit the current density at the boundaries of the emitter. These resistances show the drawback of increasing the saturation voltage of the transistor by the amount $V_{CEsat} = R_E \times I_{Csat}$.

On the other hand, the base ballast resistance is obtained through a "N^+ pocket" (in the case of NPN), around the emitter area (see Fig. 5). This N^+ diffusion, being unbiased, can't be traversed by the base current, that is therefore forced to flow below the N^+ through a small section and, in the case of a diffused base, encounters a higher resistance on the way to the edge of the emitter. In this way, it is possible to significantly improve $I_{s/b}$.

It should be noted that the SOA limits are temperature dependant and suitable derating must be applied.

Fig. 4

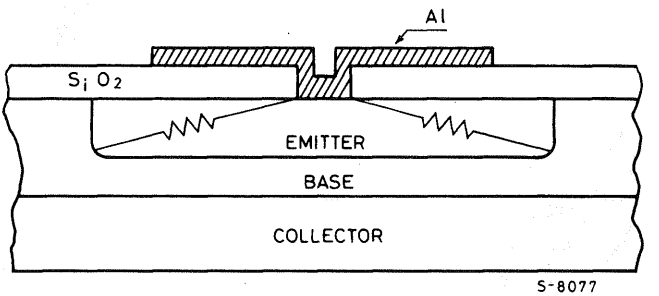
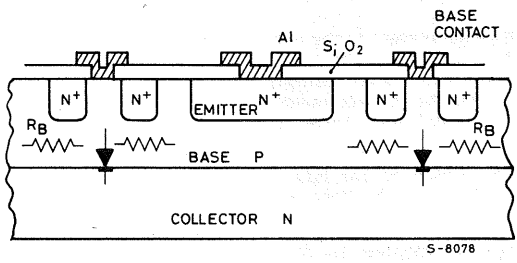


Fig. 5



REVERSE SECOND BREAKDOWN

The reverse breakdown phenomenon ($E_{s/b}$) is also due to thermal and electrical instability of the transistor. As already mentioned, it is distinguished from $I_{s/b}$ by the presence of a reverse I_B (i.e. with a direction opposite to the normal direction of a transistor operating in the active zone) and by high V_{CE} values of the transistor. The device may be in these working conditions during turn off with an inductive load.

In the following figure (Fig. 6) the common emitter characteristic curves for a transistor are shown.

Fig. 6

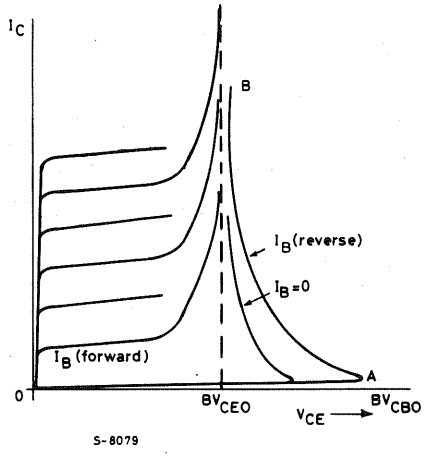


Fig. 7

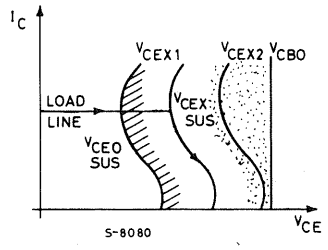
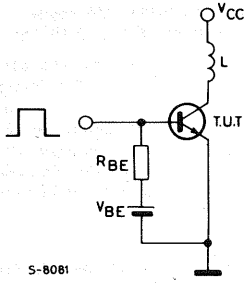
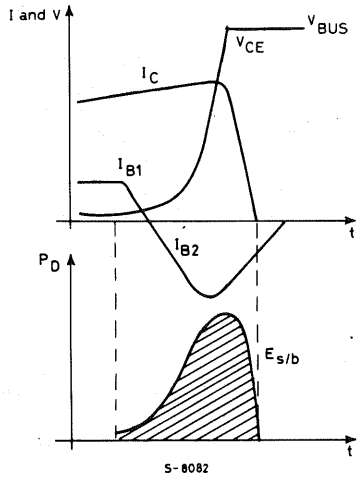


Fig. 8





It may be easy to understand the behaviour of these curves when the common emitter gain expression is considered:

$$h_{FE} = a_F/1 - a_F \qquad (1)$$

for high V_{CE} values, a_F is replaced with M x a_F.

For low V_{CE} values, M is an insignificant factor, being very close to 1. M increases when V_{CE} is increased according to the following expression:

$$M = \frac{1}{1 - (V_{CE}/BV_{CBO})^n} \quad (2)$$

From expression (1) and (2) it is evident that h_{FE} depends on V_{CE}, becoming infinite when $M \times a_F = 1$ (BV_{CEO}).

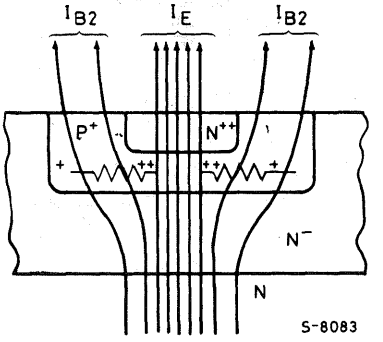
The negative slope section, which is a feature of the curves with $I_B < 0$ is due to the fact that a_F decreases at low values of the emitter current.

During turn off with an inductive load, the transistor has to operate with negative base current and a high value of I_C. It has often to reach a working area above V_{CEO}, remaining there all the time required for the inductance to be discharged (see Fig. 7). Fig. 8 shows the behaviours of I_C, V_{CE}, I_B and the power dissipated by the transistor during turn off.

The area of the dissipated power corresponds to the energy stored by the inductance $1/2 \times L \times I^2$, which is discharged into the transistor and this is called second breakdown energy ($E_{s/b}$).

Similary to $I_{s/b}$, the voltage drop due to the reverse I_B flowing through the side resistance rbb' makes the centre of the emitter strip more biased than its periphery (Fig. 9). In this way, a current concentration occurs at the emitter centre.

Fig. 9



Let's analyse the case of an NPN transistor with diffused base and epitaxial collector, i.e. with constant concentration ND of donors doping particles.

Poisson's equation is recalled below:

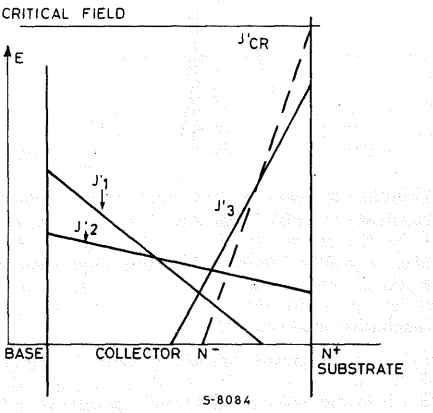
$$\frac{\partial E}{\partial X} = -\frac{\partial^2 V}{\partial X^2} = \frac{\rho(x)}{\epsilon} \quad (3)$$

The X axis is normal to the silicon dice surface, ρ (x) is the charge per unit volume, ϵ is the dielectric constant of silicon. When the collector current is limited to low values, expression (3) becomes (q being the electron charge):

$$\frac{\partial E}{\partial X} = \frac{qNo}{\epsilon} \quad (4)$$

and the electric field behaviour is similar to that shown in figure 10 for $J_C = J'_1$.

Fig. 10



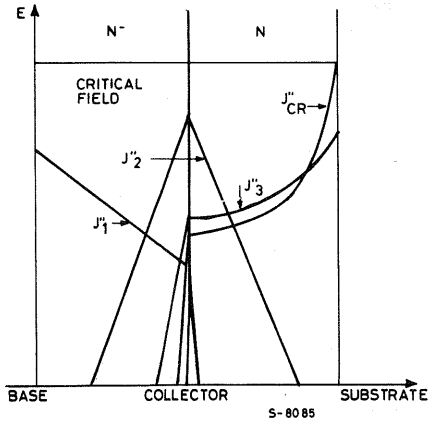
The voltage V_{CB} (= V_{CE}) is that given by the area of the E-X graph and is smaller than primary breakdown voltage, due to the reaching of critical field E_{cr}. In the presence of signigicant values of current density J_C, the expression (4) is modified due to the n concentration of electrons flowing at the speed V through the depletion layer.

$$\frac{\partial E}{\partial X} = \frac{q(ND - n)}{\epsilon} \quad \text{where } n = \frac{J_C}{qV} \quad (5)$$

At constant V_{CB}, the area limited by E has to remain constant. When J_C increases, the E-X slope varies (J'_2) until its sign is changed (J'_3) and E_{cr} is reached (J'_{cr}). At this point avalanche multiplication occurs locally of electron - hole pairs with an uncontrolled current increase and so a strip is formed with a very high temperature that gives rise to either cristal damage or silicon melting. Possible crystal defects, metal ions, junction disuniformities just further exagerate this phenomenon. The avalanche multiplication is a very fast and very localized process, therefore the device remains externally cold. The $E_{s/b}$ behaviour isn't practically influenced by the die bonding quality. High $E_{s/b}$ values can be obtained with a proper design of geometry, to limit the current crowding and, most of all, by inserting a second epitaxial layer N of intermediate doping between the collector and the substrate.

The intermediate layer creates the condition shown in Fig. 11. When the current density increases (J'_2) the electric field at the interface N^-/N is in-

Fig. 11



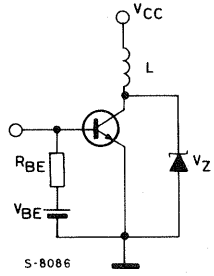
creased. Anyway, before the critical field E_{cr} is reached at this interface, the contribution of layer N becomes significant in sustaining the voltage. A further density increase (J'_3) reduces the electric field at the interface N^-/N and the breakdown isn't triggered until the critical field is reached at interface N/N^+.

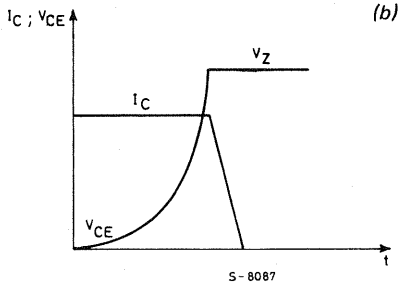
For a good power transistor with $V_{CEO(sus)}$ = 450V the current density J'_{rc} corresponding to E_{cr} is in the order of 20A/mm², greater by a factor 10 when compared to the average current density, given by the ratio between maximum saturation current and emitter area.

The $E_{s/b}$ behaviour is also influenced by the conditions outside the transistor, R_{BE}, V_{BE}, L.

The base conditions are especially important, as they regulate the crowding phenomenon.

Fig. 12





The most commonly used system by power designers to reduce the $E_{s/b}$ effect during turn off with inductive load is a clamping or 'snubber' circuit, that limits the voltage peak between collector and emitter.

The presence of the clamping circuit (in Fig. 12 for sake of simplicity it is schematized with a zener diode) allows only a minimal amount of the energy stored in the inductance to be absorbed by the transistor, and $E_{s/b}$ becomes independent of the value of L and practical RBSOA limits may be defined.

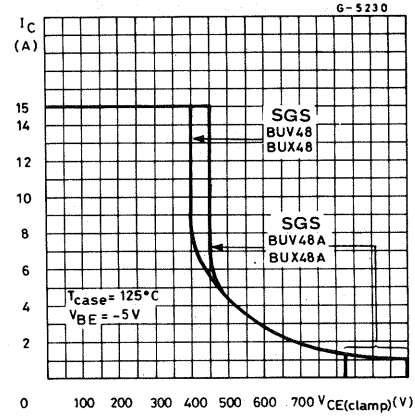
It must be noted anyway that the presence of high V_{CE} and negative I_B current may give rise at high current to the previously described $E_{s/b}$ phenomenon, even in the presence of the clamping circuit.

The multiepitaxial transistors show a better behaviour even in the presence of a clamp.

The reverse bias safe operating area (Fig. 13) establishes the maximum switchable current with inductive load versus clamping voltage in very harsh base conditions that simulate the real base driving conditions in the circuits.

Note that the temperature is not a major factor in the $E_{s/b}$ and so the RBSOA rating can be considered to be independant of temperature.

Fig. 13



CONCLUSION

Second breakdown performance is a function of transistor technology and cannot always be improved without some trade-off in other parameters. The application conditions have a considerable effect on both $I_{s/b}$ and $E_{s/b}$ capability.

AN INTRODUCTION TO POWER MOS

A POWER MOS transistor is a power transistor produced with MOS, and not the usual bipolar technology.

Special characteristics are higher switching speeds and easier driving. This intruductory note describes the essential points of the MOS structure when used for power devices.

WHAT DOES MOS MEAN ?

It means that the essential part (the silicon chip) of the device is made up of three layers:

- one conductive layer (M for metal) that is the control (drive) electrode
- one isolating layer (O for oxide) that prevents any current flow from the drive electrode to the other two electrodes, but does not block the electric field
- one semiconductor layer (S for semiconductor) which switches on or off depending on the electrical field imposed on it by the control electrode through the opening in the P zone of a conductive channel between the two zones.

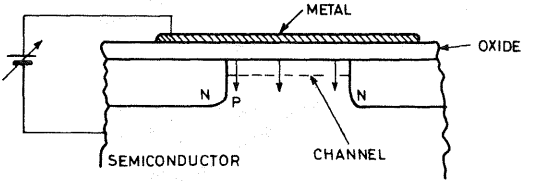
WHAT DOES POWER MOS MEAN ?

Fig. 1 shows that the device is totally implemented on the chip surface. In other words both the on and off states are implemented in a horizontal plane:

- the ON STATE i.e. the residual resistance when in the on state corresponds to conduction on the top surface of the silicon
- the OFF STATE i.e. the depletion region of one of the two PN junctions, with its resistivity and length, gives the device its voltage rating.

With the present technology the "on the surface" approach allows the production of MOS transistors

Fig. 1 - MOS basic structure



that can handle tens of volts and miliamperes (as in MOS microprocessors or in MOS memories). A power transistor must be able to handle no less than a few amperes at voltages of 50-100V or higher. The approach of several devices "on the surface" connected in parallel is unsuitable due to the problems of excessive connections, as each cell would have three terminals.

The best solution is to exploit the semiconductor both vertically as well horizontally. The paralleling of one of the two N doped regions of all the elementary structures in parallel occurs on the bottom face of the semiconductor.

At the same time, the PN junction that implements the off performance (its length corresponds to the voltage rating of the device) can be positioned vertically, and so avoiding the waste of horizontal space. The channel must be short (1 to 2 microns) to obtain characteristics of practical interest.

As a result, the POWER MOS device consists of multi - MOS basic cells, with all the N^+ type SOURCE zones connected in parallel on the top side of the semiconductor chip, as are the cell GATES. The common substrate of the chip forms the DRAIN.

Fig. 2 - V-Groove structure

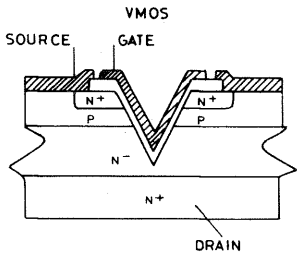


Fig. 3 - U-Groove structure

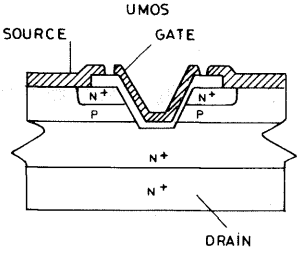
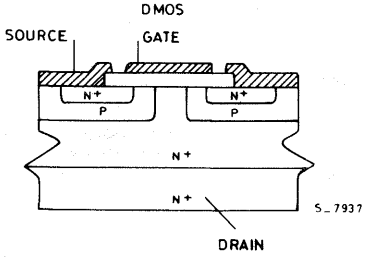


Fig. 4 - D-MOS structure

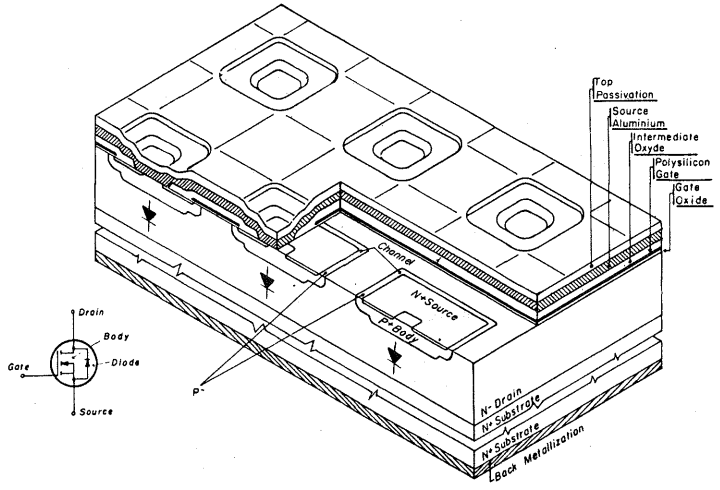


THE POSSIBLE STRUCTURES

Figures 2, 3 and 4 show the chronological progression of the different solutions used in the industry to implement the elementary POWER MOS structures.

The P doped semiconductor area that appears on the surface of the semiconductor in front of the metal electrode is the channel. There is an N^-

Fig. 5 - SGS POWER MOS cell structure



layer with low doping (high resistivity) on one side of the channel. This N layer becomes depleted when the voltage is applied to the device, and consequently allows the device to sustain applied voltages without reaching too high an electric field at any point of the chip.

Reaching the critical field means reaching the point of voltage breakdown (primary breakdown).

"V" and "U" type structures have been abandoned because the production process is both difficult and critical. Nowadays practically all POWER MOS are of the D type as shown in Fig. 4. D as a prefix means that the channel is produced by diffusion.

All the devices have in common the fact that the current traverses the device vertically, as a consequence two electrodes appear on the surface:

- SOURCE
- GATE

and one electrode appears on the bottom:

- DRAIN

Fig. 5 shows the actual structure of an SGS POWER MOS in an expanded view of a piece of the chip. All the important elements can be located in the figure.

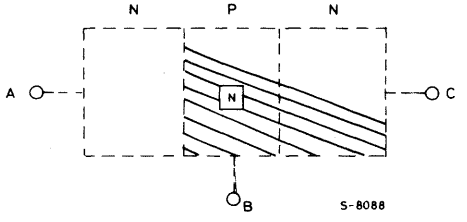
HIGH VOLTAGE POWER MOS

One of the most important questions the circuit designers ask POWER MOS manufactures is: "Why do you have very high voltage bipolar devices but not high voltage POWER MOS?".

To answer this question it is useful to remember an important phenomenon that appears in a bipolar device and not in a POWER MOS device.

Fig. 6 A schematic diagram of a bipolar device in the saturation region.

Fig. 6



The N collector is invaded by the N carriers coming from the base and its resistivity is modulated. The resistivity of the N collector layer is greatly reduced due to the invasion of these minority carriers.

A bipolar transistor is fully saturated when the minority carriers from the base have totally invaded the collector. For both bipolar and SGS POWER MOS devices the collector is an epitaxial silicon layer of high resistivity. Its thickness, and consequently its no-current resistance, corresponds to the voltage rating of the device.

Since a SGS POWER MOS device is a unipolar (majority carrier) by definition it is very fast in switching.

As a consequence in a POWER MOS there is no modulation of the conductivity and the drain resistivity remains at the same value as its epitaxial specification implies.

The current flows through two resistances:

1) Resistance of channel (R-channel)
2) Resistance of drain (R-drain)

So, if the two devices have:

- similar epitaxial spec, to guarantee the same breakdown voltage (BV_{CES} for BIPOLAR, $V_{(BR)DSS}$ for POWER MOS)
- same chip area, to guarantee the same current flow they will show the following output characteristics (Fig. 7).

Fig. 7a - POWER MOS SGSP361 $V_{(BR)DSS}$ = 100V

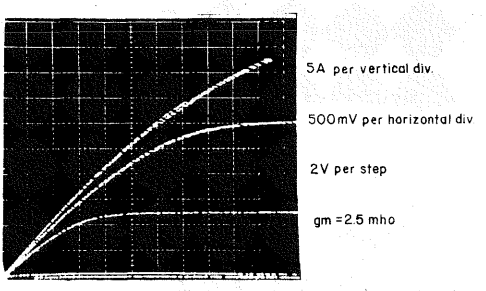
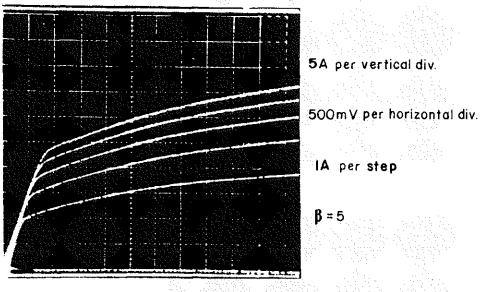
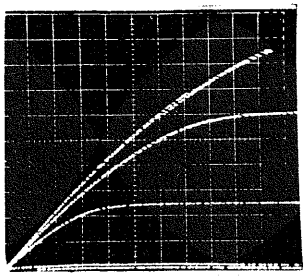


Fig. 7b - BIPOLAR 2N5039 (BV_{CEO} = 75V, BV_{CES} = 120V, same die size)



The voltage drop in SGS POWER MOS is greater than in bipolar devices. If the thickness of the epitaxial layer is increased to raise the breakdown voltage, this is partially compensated by the conductivity modulation phenomenon in the bipolar devices while in POWER MOS this cannot occur.

Fig. 8 - Shows the output characteristics for POWER MOS: SGSP361 V(BR)DSS = 100V SGSP363 V(BR)DSS = 200V, same die size.



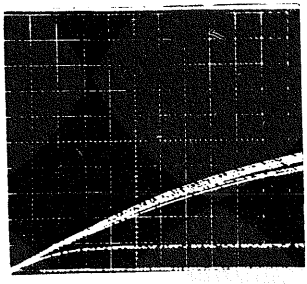
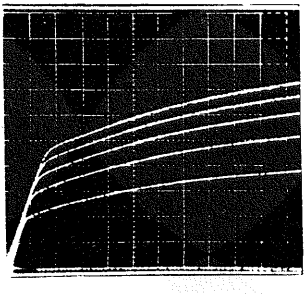
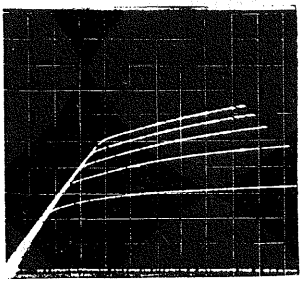


Fig. 9 - Shows the output characteristic for BIPOLAR: 2N5039 (BVCEO = 75V, BVCES = 120V), BUX41N (BVCEO = 160V, BVCES = 220V, same die size)





In an SGS POWER MOS the increase of the voltage drop - due to the increase of $R_{DS(on)}$ is much more accentuated than in a bipolar device. It is possible to describe the increase of $R_{DS(on)}$ versus the breakdown voltage using the following law:

$$R_{DS(on)}(V) = R_{DS(on)}(Vo) \times \left(\frac{V}{Vo}\right)^{k}$$

where K is a coefficient whose value depends on the voltage values at which the comparison is made:

K = 1.8 at low voltage (50-100V)

K = 2.5 at high voltage (500V)

K = 2.7 at voltages higher than 500V

To increase the SGS POWER MOS breakdown voltage from 500V to 1000V we have to compute:

$$R_{DS(on)}(1000V) = R_{DS(on)}(500V) \times \left(\frac{1000V}{500V}\right)^{2.7} = 7.3 \times R_{DS(on)}(500V)$$

To compensate for the increase of $R_{DS(on)}$ it is necessary to increase the chip area at least two or three times. This leads to the following problems:

1) The chip is much more expensive. For the same chip area a SGS POWER MOS is more expensive than a bipolar, it is easy to understand that if the die size were increased the SGS POWER MOS would be even more expensive.
2) The above solution could only be used for small chips, because if big chips were further enlarged they would be too big to produce and assemble.
3) The device would be difficult to drive. In fact the greater the chip area the greater the input capacitance of the device. To charge and discharge this capacitance, it is necessary to supply high current peaks at the gate.

So in the range of high voltage applications bipolar devices will continue to be used in the future, while SGS POWER MOS will be used much more frequently in low to medium voltages and very fast switching applications where the benefits of lower switching losses compensate the higher device cost.

COMPARISON OF SGS POWER MOS AND BIPOLAR POWER TRANSISTORS

It is highly predictable that in the near future SGS POWER MOS will, in many applications, gradually replace power bipolar devices due to the numerous advantages they offer.

Table 1 lists the principal differences between SGS POWER MOS and bipolar transistors. In addition to their inherent high switching speed resulting from the lack of minority carrier injection during operation, SGS POWER MOS with their insulated gates require negligible input gate-drive current. Other advantages are related to the negative temperature coefficient of their current, which prevents the formation of thermal instabilities and makes the paralleling of devices much more reliable. In contrast, bipolar transistors require ballasting or careful device matching to prevent thermal runway.

Only in high voltage cases is SGS POWER MOS on-resistance higher than in bipolar transistors.

This leads to slightly larger steady state power dissipation and could offset the advantages. The prospects for SGS POWER MOS appear bright in many high frequency applications where switching losses become very high for bipolar devices.

Table 1 - Comparison of MOS and bipolar power transistors

MOS	BIPOLAR
Majority-carrier device	Minority-carrier device
No charge-storage effects	Charge stored in the base and collector
High switching speed less temperature sensitive than bipolar devices	Low switching speed temperature sensitive
Drift current (fast process)	Diffusion current (slow process)
Voltage driven	Current driven
Purely capacitive input impedance; no dc current required	Low input impedance; dc current required
Simple drive circuitry	Complex drive circuitry (resulting from high base-current requirements)
Predominatly negative temperature coefficient of drain current	Positive temperature coefficient of collector current
No thermal runaway	Thermal runaway
Devices can be paralleled with some precautions	Devices cannot be easily paralleled because of V_{BE} matching problems and local current concentration
Less susceptible to second breakdown	Susceptible to second breakdown
Square-law I-V characteristics at low current; linear I-V features at high current	Exponential I-V characteristics
Greater linear operation and fewer harmonics	More intermodulation and cross-modulation products
High-on resistance and, therefore, larger conduction loss	Low on-resistance (low saturation voltage) because of conductivity modulation of high resistivity drift region
Drain current proportional to channel width	Collector current approximately proportional to emitter stripe length and area
Low transconductance	High transconductance
High breakdown voltage as the result of a lightly doped region of a channel-drain blocking junction.	High breakdown voltage as the result of a lightly doped region of a base collector blocking junction.

PERFORMANCE COMPARISON

At this point a comparison between SGS POWER MOS and bipolar devices can be made in order to evaluate their switching speeds which give an indication of the energy consumption during transitions, and their different values of $V_{DS(on)}$ and V_{CEsat} related to energy consumption during the on state.

The two devices used in the comparison are:

SGSP565: SGS POWER MOS; 400V; 6A
$R_{DS(on)} = 1\Omega$

SGSD00036: SGS BIPOLAR; 400V; 6A
(very fast switching)

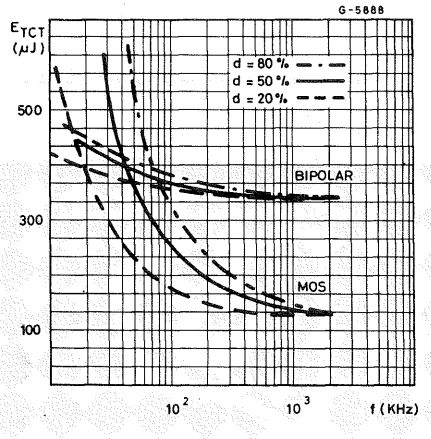
$V_{DD}/V_{CC} = 200V$
$I_L = 5A$ (average value)

Since the input losses were neglected the bipolar devices have an advantage in this comparison.

E_{TOT} (the energy losses per cycle) as a function of

the operation frequency, for different values of the duty cycle can be seen in Fig. 1. For a bipolar device, the energy used during the on phase has only a slight influence with frequency variation. SGS POWER MOS however are influenced by these variations, and as a result two curves, relative to the same duty cycle, are obtained. The intersecting points of these curves can be considered as a guideline to the use of the devices.

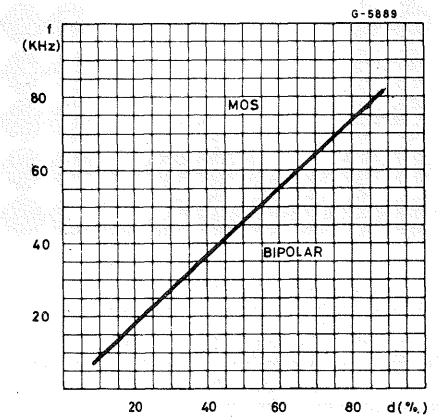
Fig. 1 - ETOT versus frequency (kHz)



In order words if both the duty cycle and the power to be switched are fixed there is a frequency value above which the dissipated energy per cycle for an SGS POWER MOS transistor is less than for a bipolar device. This means the higher the frequency the more advantageous it is to use a SGS POWER MOS.

Under relatively low frequency conditions the value of the duty cycle "d" is fundamental in determining the advantages of both bipolar and SGS POWER MOS technologies. From the graph in Fig. 2 the best working conditions for both devices can be seen.

Fig. 2

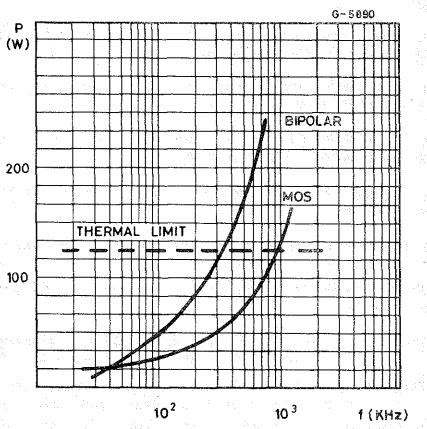


A SGS POWER MOS is most suited to high frequency conditions (> 100KHz) for any given value of "d". Maximum frequency limitations are of a thermal nature only and depend on the die size.

For the SGS POWER MOS under consideration the maximum power dissipated is 100W when $R_{thj\text{-}case} = 1°C/W$ and $T_{jmax} = 150°C$.

By plotting the power dissipated as a function of the frequency, when d = 50% the actual limits of the two technologies can be seen (Fig. 3).

Fig. 3



THERMAL STABILITY

The greater thermal stability of SGS POWER MOS with respect to bipolar devices is essentially due to the different response that the two devices exhibit when they are subjected to external power pulses.

The intrinsic mechanism which could lead to thermal runway in a bipolar and in a SGS POWER MOS device, are as follows.

In a bipolar device an external power pulse results in an increase in the junction temperature (T_j). This causes V_{BE} to decrease and h_{FE} to increase. Both cause the collector current to increase and this consequently further increases T. This positive feedback is compensated only by the base widening effect at high currents (that is a higher recombination of the minority carriers). At high voltages the base widening effect is not present so that any hot spots lead to thermal runaway.

These phenomena, if not controlled, could seriously damage a bipolar device.

A power pulse in an SGS POWER MOS device would cause:

1) an increase in temperature of the device
2) a decrease in the threshold voltage

$$V_{GS(th)} = V_{GS(th)}\ (25°C) \times [1 - \alpha (T - 25°C)]$$

where alpha is a positive coefficient of temperature ($\alpha = 2.10^{-3}\ °C^{-1}$).

This is positive feedback, similar to a decrease of V_{BE} in bipolar devices.

But in a SGS POWER MOS device there is also a very important negative feedback. That is an increase of $R_{DS(on)}$ with temperature:

$$R_{DS(on)}(T) = R_{DS(on)}(25°C) \times [1 + \alpha(T-25°C)]$$

where alpha is the temperature coefficient (alpha = $8 \cdot 10^{-3}$ $°C^{-1}$). The effect of a increase in $R_{DS(on)}$ is greater than the variation in $V_{GS(th)}$. As a result SGS POWER MOS devices are thermally stable. The difference in behaviour of the two devices is even more exaggerated when dealing with paralleled chips.

Two comparisons between bipolar and SGS POWER MOS devices have been made.

The first deals with the bahaviour of single chips in SOT-93 (TO-218) package.

The SGS POWER MOS used in this test is the SGSP475 (400V, 12A, 0.55Ω).

The power bipolar device used in the BUV48 (400A, 10A).

The parameter used to measure the thermal imbalance of the devices is the variation of the thermal resistance $R_{thj\text{-}case}$ due to an external power pulse.

In fact an increase of $R_{thj\text{-}case}$ implies a decrease of the active area of the chip and therefore a disuniformity in the spreading of the heat, with a creation of hot spot and thermal and electrical unbalancing. The devices have been tested under several conditions, with respect to the power dissipation and the voltage across them (V_{DS} for SGSP471, V_{CE} for BUV48). The results are shown in Fig. 4 and Fig. 5).

SGSP475 shows optimum thermal stability under all conditions while bipolars, with V_{CE} = 45V and P > 45W, show a degrading of the thermal performances.

The best electrical and thermal performances of the SGS POWER MOS are confirmed by the thermal maps which show a uniform distribution of heat under different working conditions (Fig. 6 and 7).

Fig. 4 - Variation of $R_{thj\text{-}case}$ vs. P (POWER MOS) SGSP475 SOT-93

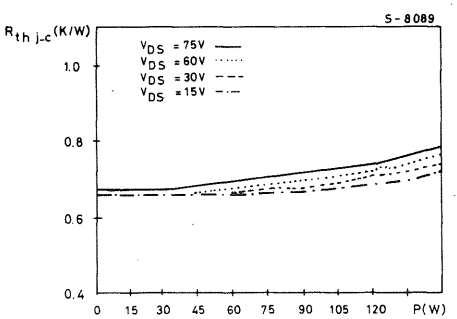


Fig. 5 - Variation of $R_{thj\text{-}case}$ vs. P (BIPOLAR) BUV48 SOT-93

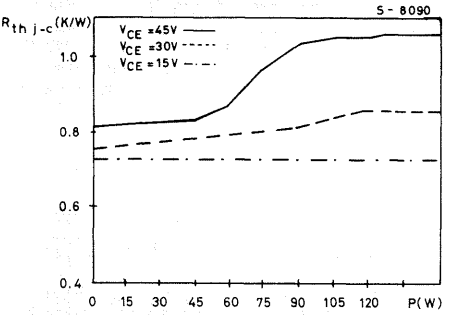


Fig. 6

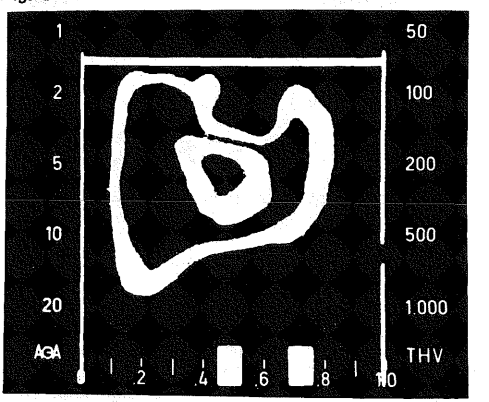
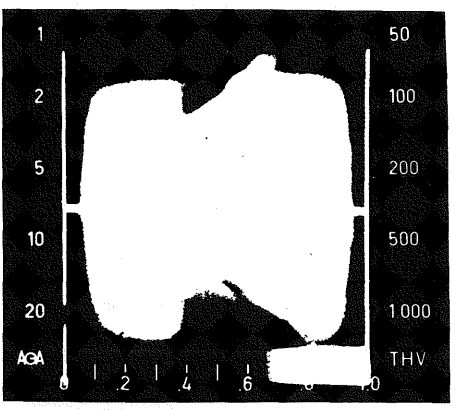


Fig. 7



It is only at V_{DS} = 75V that is it possible to notice a slight variation in the working temperature.

The thermal instability has a greater effect when the die are assembled in parallel since any unconformity would be enhanced leading to an overloading of some of the die.

The second thermal comparison was made between SGS POWER MOS and bipolar devices in multiple chips mounted in a parallel configuration.

The SGS POWER MOS device under test was:

SGS30MA050D1: four SGS POWER MOS chips paralleled in TO-240 a package I_{DMAX} = 30A, V_{DSS} = 500V, $R_{DS(on)}$ = 0.250Ω.

The bipolar device under test was:

SGS40TA045D: four bipolar chips paralleled in TO-240 package I_C = 40A, V_{CEO} = 450V

The results are shown in Fig. 8 and 9 and reveal a much better thermal stability for the SGS POWER MOS than for the bipolar device.

Fig. 8 - Variation of $R_{thj\text{-}case}$ vs. P (POWER MOS) SGS30MA050D TO-240

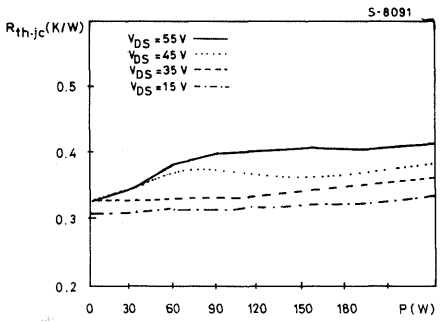
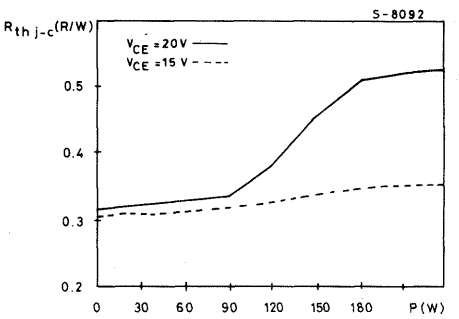


Fig. 9 - Variation of $R_{thj\text{-}case}$ vs. P (BIPOLAR) SGS400TA045D TO-240



SGS POWER MOS IN SWITCHING AN EVALUATION METHOD AND A PRACTICAL EXAMPLE

INTRODUCTION

SGS POWER MOS are used in switch mode power supplies, H.F. welding systems, industrial ovens, relay drivers and other similar applications. These diverse applications of SGS POWER MOS in the field of control is due largely to their ability to handle high power at very high switching speeds up to hundreds of kHz.

The great improvement in the ability to switch power using SGS POWER MOS is due to the recent progress made in the manufacture and technology of semiconductors. This ability to produce power devices using MOS technology has opened up a new fields of applications. In POWER MOS devices the flow of current from the drain to the source is voltage controlled. Consequently the energy consumed in driving the device is much less than for a bipolar device. SGS POWER MOS devices are unipolar and do not make use of minority carriers for conduction. This makes them very attractive to use in power switching at very high frequencies.

SWITCHING PHASE

In pratical working conditions three main phases can be distinguished:

On state

When the device is on and the channel open, the dissipated power is:

$$P_{on} = V_{DS\,(on)} \times I_D \quad (P_{on} = V_{CEsat} \times I_C \text{ for bipolar transistors})$$

It can be reduced optimizing the technology (metal back, epitaxial thickness) and the design (cell dimensions and layout).

Off state

When the device is off and the drain is at the battery voltage, the power dissipation is:

$$P_{off} = V_{DD} \times I_{DSS} \quad (P_{off} = V_{CC} \times I_{CEX} \text{ for bipolar transistors})$$

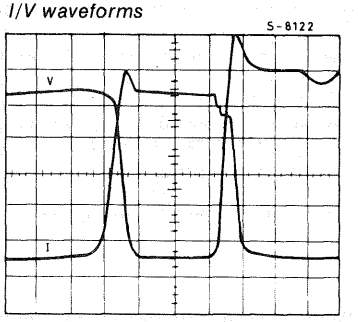
"TRANSITIONS"

During switching the dissipated power instant by instant is:

$$P = V_{DS} \times I_D$$

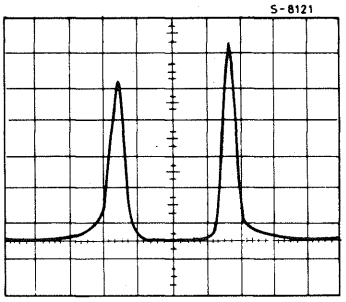
and depends on the on/of switching speed of the device as can be seen in Figs. 1 and 2.

Fig. 1 - I/V waveforms



t: 100 ns/div, V: 45V/div, I: 1.2A/div, Vg=10V, Rg=25Ω

Fig. 2 - Power dissipation waveforms.



t: 100 ns/div, P: 200 W/div, Vg=10V, Rg=25Ω.

Q. THE EFFICIENCY FACTOR

The performance of an SGS POWER MOS device can therefore be rated as the ratio between the total power in switching-on and off and the energy dissipated per cycle. It can be expressed as:

$$Q = \frac{P_t}{E_{on} + E_{off} + E_p}$$

Where:

E_{on} - is the energy lost in the turning-on and on phases

E_{off} - is the energy lost in the turning-off and off phases

E_p - is the energy lost to drive the circuit.

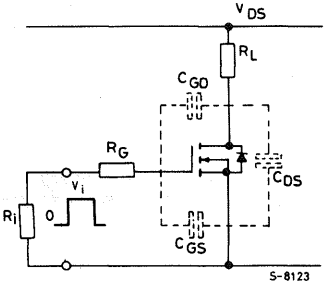
The quantity Q is a frequency and is an index of the maximum frequency at which the device can most efficiently operate, considering P_t as the maximum power that the device can dissipate in practical working conditions.

To fully understand this equation a brief analysis of switching phenomena is essential. As previously mentioned, SGS POWER MOS do not make use of minority carriers for conduction. The recombination of these minority carriers is a switching speed limitation. In SGS POWER MOS devices the majority carrier flow is simply controlled by the gate voltage and therefore its switching speed is limited only by the time needed to charge and discharge the parasitic input capacitances. Consequently the switching behaviour is a function only of the ability of the driving circuit to charge and discharge some hundreds of picofarads. This is why SGS POWER MOS can switch so fast - in the range of tens of nanoseconds.

INPUT

SGS POWER MOS devices behave quite differently from bipolar power devices, as far as the driving energy is concerned. SGS POWER MOS require driving power during the charge and the discharge phases of the input capacitances. Fig. 3 shows an SGS POWER MOS driven by a voltage generator with an internal resistance R_i and an open circuit voltage V_i, where R_L is the load.

Fig. 3 - SGS POWER MOS equivalent circuit.



The input capacitance $C_{iss} = C_{GS} + C_{GD}$ during the switching cycle is not constant for two reasons.

1) C_{GD} can be seen as the capacitance between the gate electrode and the drain, where the dielectric is the depleted drain layer. The drain epi-layer is fixed, but its depleted part varies according to V_{DS}. The higher V_{DS}, the thicker the depleted layer and consequently the lower the associated capacitance.
2) A more pronounced effect comes from the fact that the voltage across C_{GD}, when the gate source voltage rises from zero to its final value, V_{DS} must go down from V_{DD} to $V_{DS(on)}$. In particular C_{GD} is seen as a higher equivalent capacitance during the drain 'on' transitions. The input must be fed a charge:

$$Q = C_{GD} (V_{DD} - V_{DS(on)})$$

to account for the voltage variation across C_{GD}. This happens when the gate voltage reaches $V_{GS(th)}$, the threshold voltage, and the drain voltage starts falling. It is not until the required charge Q is provided that V_{GS} can increase. This is called the Miller Effect. For a while the equivalent input capacitance appears infinite and V_{GS} remains at $V_{GS(th)}$ while C_{GD} absorbs the whole input current. From the moment V_{DS} reaches $V_{DS(on)}$ the input equivalent capacitance is:

$$Ceq = C_{GS} + C_{GD} \text{ (low voltage)}$$

and the transition of the output is completed. V_{GS} increases again, tending towards V_i.

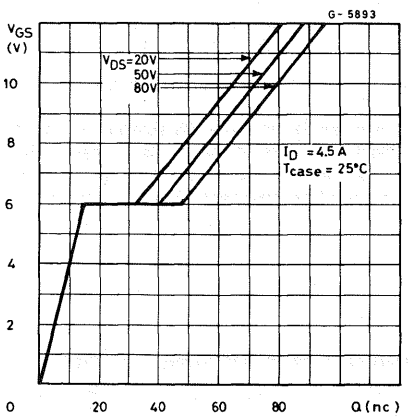
These two phenomena become apparent when looking at the gate charge versus gate source voltage diagram in the data sheets.

The diagram for SGSP471 in fig. 4 can be taken as an example.

A true capacitor would appear as a straight line starting from the origin. In fact the first segment corresponds to an equivalent capacitance:

$$C_{eq} = C_{GS} + C_{GD} \text{ (high voltage)}$$

Fig. 4 - Gate charge vs, gate-source voltage SGSP471



The horizontal segment corresponds to an equivalent infinite capacitance i.e. the charging of C_{GD} with the gate at V_{th} and the drain falling from V_{DD} to $V_{DS(on)}$. The last segment has a slope corresponding to a capacitance:

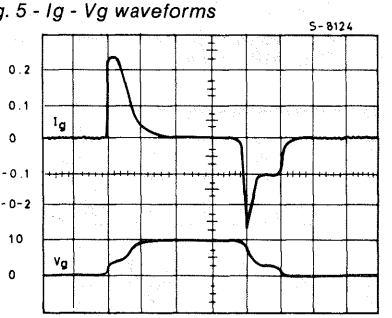
$$C_{eq} = C_{GS} + C_{GD} \text{ (low voltage)}$$

The difference in slope of the first and third segment shows how C_{GS} differs in the two cases.
The behaviour at turn off of the input capacitances is exactly opposite, where the described phenomena occur in reverse order. At this point the energy drive required to make the SGS POWER MOS switch can be calculated as:

$$E_p = 1/2 C_{eq} \times V_{GS}^2 = 1/2 Q_G \times V_{GS}$$

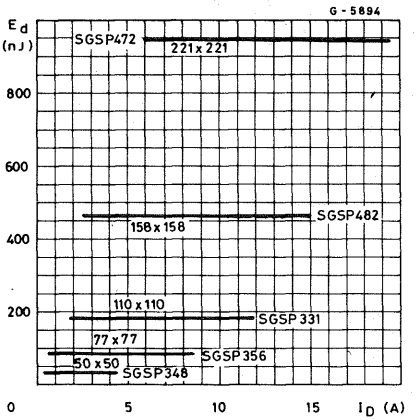
Q_G and V_{GS} can be obtained from fig. 4.
The input energy can also be obtained in a more direct manner by calculating the integral of the I_G wavefrom during the turn-on or turn-off phase, the two areas being equal (see fig. 5). In fact this integral represents the quantity Q_G (gate charge) which in turn permits the calculation of E_p.
The values of E_p have been calculated for all SGS POWER MOS in the present product range. They are a function of the die area only, for a given supply voltage V_{DD}, and have been represented for different die areas as a function of I_D in Fig. 6.

Fig. 5 - Ig - Vg waveforms



t: 0.5 μs/div, I: 0.1 A/div, V: 10 V/div

Fig. 6 - Ep vs I_D at $V_{DD} = BV_{DSS}/2$



The driving energy does not vary for devices with the same die area but different breakdown voltages, if their drive supply voltage has a constant ratio to their breakdown voltage.
In brief E_p can be plotted as a function of the die area, for a supply voltage equal to half the rated V_{DSS} of the device (see fig. 7). The method used here to calculate Q_G is different from that in the data sheet where Q_G is plotted as a function of V_{GS}.
As the results obtained in both methods were in good agreement the validity of the method used here is confirmed.
The driving circuit itself dissipates power to drive the SGS POWER MOS device. Current only flows in the gate circuit during turn-on and turn-off periods. This current flowing through the drive circuit will dissipated energy.
With reference to fig. 8, where the 50 ohm resistor is inserted to match the cable and the device, during the on phase, there is a constant power dissipation in the resistor R_1.

$$(V^2_{GS} / R_1) \cdot t/T$$

Where:

R_1 = 50 ohm (typical value)
t/T = duty cycle

Fig. 7 - E_p versus die side (S_q·mil)

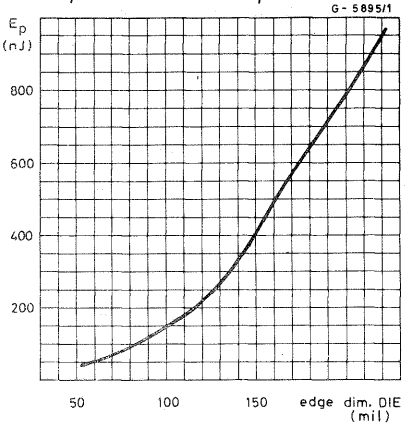


Fig. 8 - Driving circuit. A laboratory implementation

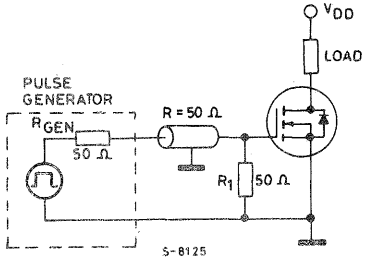


Fig. 9 - Driving circuit. A practical implementation.

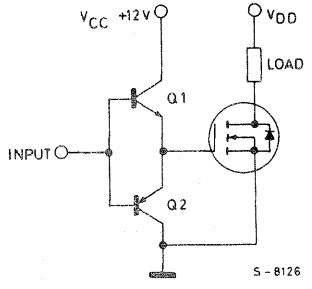


Fig. 9 shows a possible implementation that avoids steady state dissipation in the driver. The NPN transistor, Q1, only conducts at the beginning of the on phase when charging the input capacitances. Conversely the PNP transistor, Q2, only conducts at the beginning of the off phase when discharging the input capacitances. They never conduct at the same time. No conduction occurs during steady state. In addition, when either of the two transistors conduct their output impedance is very low thus improving the switching of the POWER MOS device. The total energy dissipated per cycle, in the input stage (including the SGS POWER MOS input) is:

$$E_p = Q_G \times V_{CC}$$

V_{CC} = input supply to driving stage voltage, + 12V in Fig. 7

This energy is actually dissipated in the two driving transistors, because the parasitic input capacitances of the SGS POWER MOS act as a non-dissipating element, storing energy from Q1 at turn-on, and giving it back to Q2 at turn-off.

OUTPUT

Switching times for resistive load

Fig. 10 shows the circuit used to measure the switching times of a resistive load.

Fig. 10 - Test circuit

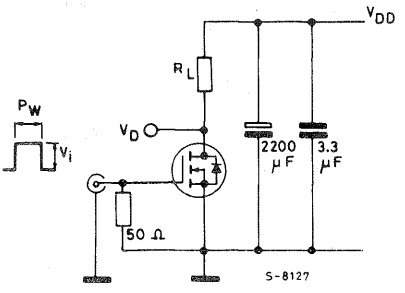
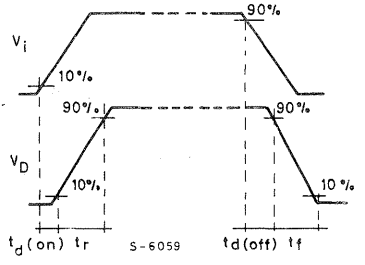


Fig. 11 - V_{GS} and V_{DS} waveforms



Turn on delay time

Turn on delay time ($t_{d(on)}$ in fig. 11) represents the time necessary for V_{GS} to reach the threshold

level V_{th} at which the device begins to conduct. The smaller the threshold voltage and the bigger the V_i value, with respect to V_{th}, the smaller the $t_{d(on)}$ value. In fact from the equation:

Eq.1 $V_{GS} = V_i (1 - e^{-t/Ri.Ciss})$.

where Ri. Ciss is a time constant and by substituting V_{GS} with V_{th} in Eq.1 we obtain:

Eq.2 $t_{d(on)} = Ri.\ Ciss\ ln \dfrac{V_i}{V_i - V_{th}}$

Considering typical values for V_i and V_{th} we have:

$$t_{d(on)} = 0.35 \times Ri.\ Ciss$$

In pratice this time is negligible (10 - 20ns) when compared to others. During this time the device is off and the energy dissipated is therefore in the order of pJ and compared with the total energy loss it can be completely neglected in this analysis.

t-RISE AND t-FALL TIMES

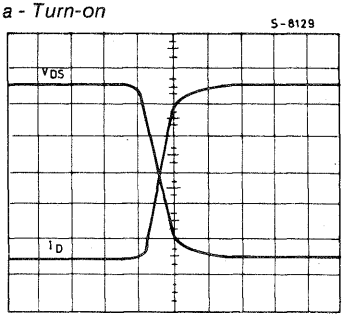
t-rise and t-fall are defined by the slopes of V_{DS} as shown in fig. 11.

Turn-off delay time

$t_{d(off)}$ can be referred to as the delay time since it represents the time necessary to remove the excess charge from the gate and channel, due to the input overvoltage.

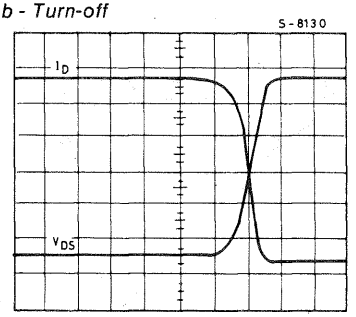
Typical drain current and voltage waveforms (t = 50ns / div.)

Fig. 12 a - Turn-on



t = 50 ns/div

Fig. 12 b - Turn-off



t = 50 ns/div

PARASITIC CAPACITANCES DURING SWITCHING CYCLES

As already mentioned the switching of an SGS POWER MOS device consists fundamentally in the loading and unloading of the input capacitor.

$$C_{iss} = C_{GS} + C_{GD}$$

From Eq.1 where $R_i.C_{iss}$ is the time constant R_i includes:

R_{gen} - the internal resistance of the generator,

R_1 - the resistor between gate and source to match the driving circuit,

R_G - the internal resistance of the gate.

Fig. 13 a - Equivalent circuit

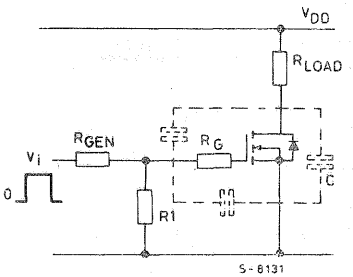
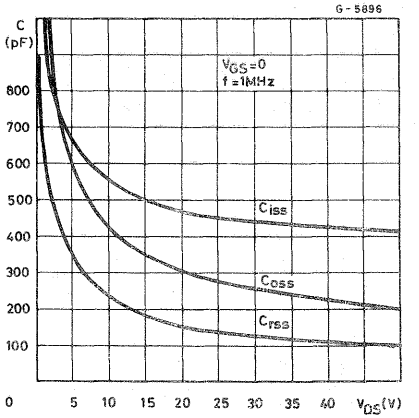


Fig. 13 b - Capacity values as a function of V_{DS}

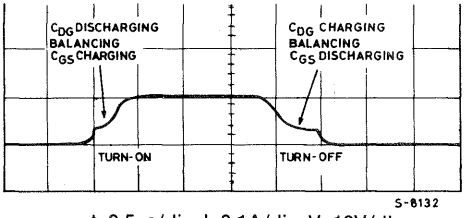


Obviously the smaller the value of Ri. C_{iss} the faster V_{GS} reaches its final value, and switches the device. To minimize this time constant the user can act on R_{gen} and R_1 and the device designer on C_{iss}.

C_{iss}, being a function of C_{GD}, varies as a function of the drain voltage as shown in the waveforms in fig. 13b and during switching it is subjected to the Miller effect. Consequently during the $t_{d(on)}$ and $t_{d(off)}$. C_{iss} remains constant, as

does the value of V_{DS}. $t_{d(on)}$ and $t_{d(off)}$ are obtained from the charging and discharging laws of a RC circuit, while during the off / on and on / off transitions, C_{iss} varies. In other words, when V_{DS} decreases during turn-on to a very low value $V_{DS(on)}$, and C_{GD} increases, there is a delay in the increase of the value of V_{GS} since the capacitor, as long as it is not charged to $V_{GS(on)}$, will absorb the gate current.
During turn-off due to V_{DS} rising the discharge current of C_{GS} will be balanced by the charging current of C_{GD}, flattening the V_{GS} curve and making it similar to that at turn-on (Fig. 13c).

Fig. 13 c - An annotated extract from fig. 5 showing the discharging and charging of C_{GD}

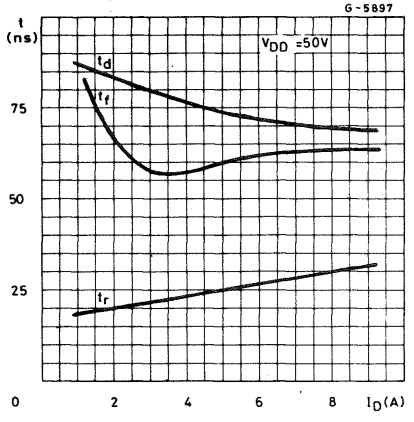


t: 0.5μs/div, I: 0.1A/div, V: 10V/div

Variations in the supply voltage V_{DD} influence these effects: the higher the supply voltage the greater the charge and therefore the t_f and driving energy required (see fig. 8 in the section OUTPUT).
Figs. 14, 15, 16 and 17 show the switching time waveforms as a function of both the supply voltage V_{DD} and the load current I_D, for two devices with different voltages and die sizes.

SGSP311	100V	7A	0.3 ohm	110 × 110 mils
SGSP369	500V	5A	1.75 ohm	156 × 156 mils

Fig. 14 - Time measurement t_d, t_f, and t_r as functions of I_D. (SGSP311)



The t_r and t_f waveforms versus V_{DD} are similar to those of E_p versus V_{DD} since they are both caused by the same phenomena. t_d is independet of V_{DD} as it is a function of C_{iss} only (which, since the Miller effect is not present, is constant during this phase).
t_d = delay time
t_f = fall time
t_r = rise time

Fig. 15 - Time measurements t_d, t_f and t_r as functions of the drain voltage for a low voltage SGS POWER MOS. (SGSP311)

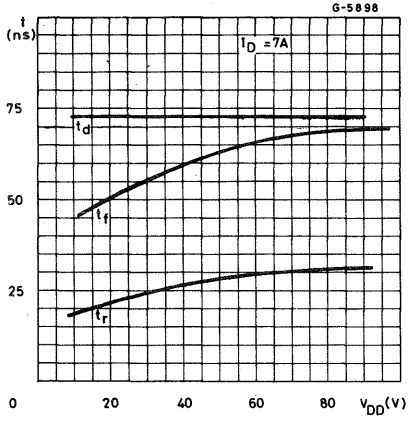


Fig. 16 - Time measurements t_d, t_f and t_r as functions of the drain current for high voltage SGS POWER MOS (SGSP365)

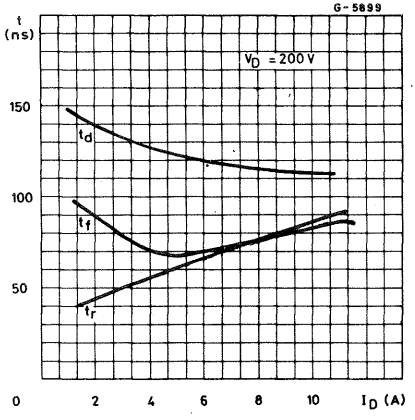
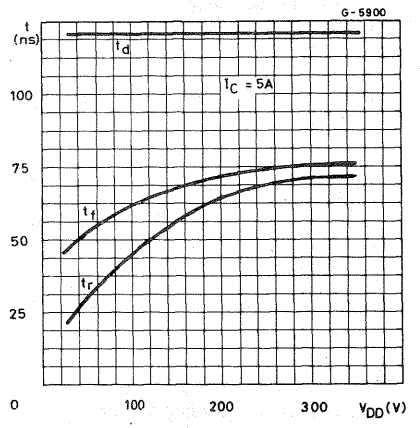


Fig. 17 - Time measurements t_d, t_f and t_r as functions of the drain voltage for high voltage SGS POWER MOS



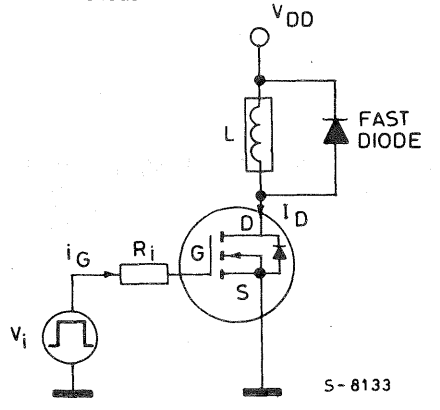
Switching times for inductive loads

In the majority of applications SGS POWER MOS are used in switching power through inductive loads (motor control, switching power supply etc.).
The fundamental objective of the device is to switch high quantities of power very quickly, in other words to maximize the ratio:

$$\frac{\text{total power switched}}{\text{energy dissipated per cycle}}$$

which depends principally on the switching times.
Understanding switching with SGS POWER MOS requires consideration of both the physical phenomenon and the energy dissipation occuring during each switching cycle.
The typical clamped inductive load circuit shown in fig. 18 is used as an example.

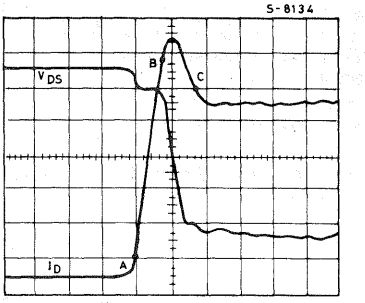
Fig. 18 - SGS POWER MOS with clamped inductive load



TURN - ON

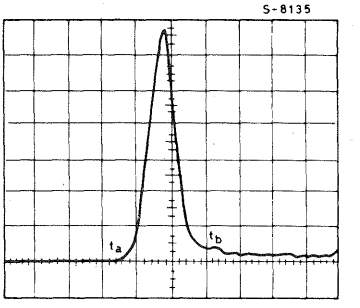
A detailed explaination of the turn-on phenomena in a SGS POWER MOS device when the load is inductive is given by Fig. 19 and 20.

Fig. 19 - Current and voltage waveforms during turn - on



t: 50ns/div, I: 1.2A/div, V: 40V/div, R=25Ω

Fig. 20 - Output energy consumption during turn-on

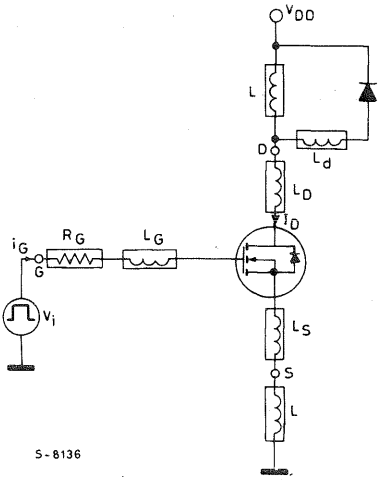


t: 50ns/div, P: 200W/div, E: 67.5 μJ

Before the turn-on phase the diode is freewheeling the load current.
Turn-on can be divided into two subphases:
1) point A to point B (Fig. 19).
Part of the current in the load (constant during the switching operations) starts to flow in the SGS POWER MOS device. The diode is recovering its reverse state. The voltage across the SGS POWER MOS device is almost equal to that of the supply since the diode still acts as a short circuit for the load at this point. There is a small step in V_{DS} waveform due to the voltage drops on the parasitic inductances L_D and L_S. The size of this step depends on the current slope dI_D/dT (L_S and L_D depend on the circuit layout).
2) point B to point C (Fig. 19).
In this phase the diode is reverse biased. The current in the SGS POWER MOS device is the sum of the current in the load plus that in the diode, which causes the peak in the I_D waveform. (see fig. 24)

The V_{DS} voltage falls to $V_{DS(on)}$ as the freewheeling diode, being reverse biased, is no longer a short circuit. However the fall of V_{DS} is delayed by the Miller effect, which increases Ciss.
All these phenomena cause a high crossover between the I_D and the V_{DS} waveforms even if the switching is very fast. In Fig. 20 the output energy consumption per turn-on phase is represented. To decrease this energy, the d_{ID}/dt (A-B phase) and the reverse recovery of the freewheeling diode (B-C phase) must be improved.
- IMPROVING d_{ID}/dt
Reference to the circuit in Fig. 21 shows the controlling parameters for d_{ID}/dt.

Fig. 21 - Circuit which includes the parasitic inductances



In this circuit the following elements have been taken into consideration:
L_d - is the parasitic inductance due to the connections between the clamping diode and the load.
L_D - is the parasitic inductance between the drain of the SGS POWER MOS device and the load.

L_G - is the parasitic inductance between the gate and the driving circuit.
L_S - is the parasitic inductance between the source and the ground.
The equation that applies to the input loop is:

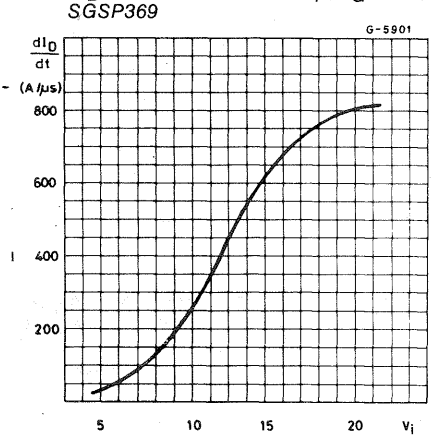
$$V_i = R_i \times i_G + L_G\, di_G/dt + V_{GS} + L_S\, dID/dt$$

Where R_i is the equivalent resistance of the driving circuit. When considering the phase when I_D increases it is possible to neglect the term $L_G\, di_G/dt$ as $di_G/dt = 0$.
During this phase the threshold voltage has already been overcome, i_G is constant. In addition V_{GS} follows the law of charging a constant capacitance. The Miller effect is not present as V_{DS} is constant.
It follows that:

$$dI_D/dt = \frac{V_i - R_i \cdot I_G - V_{GS}}{L_S}$$

and dI_D/dt can be improved by increasing V_i and decreasing R_G and L_S.

Fig. 22 - dI_D/dt as a function of V_i (R_G=25Ω) for SGSP369



Improving the reverse recovery of the diode

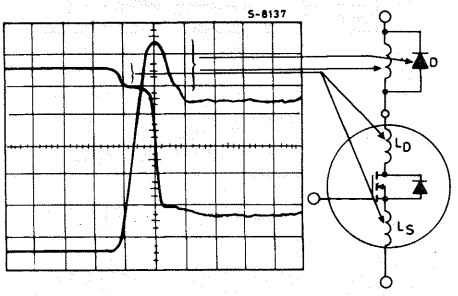
As previously mentioned, the clamping diode plays an important role in determining the waveforms of I_D at turn-on; the faster the diode, the lower the current peak in the SGS POWER MOS, the lower the reverse recovery time of the diode (t_{rr}) and the energy consumption. For this reason fast recovery diodes are typically used in these circuits.
SGS is developing a wide range of fast recovery diodes whose target characteristics are shown below (fig. 23).

Fig. 23 - SGS Fast recovery diodes

DEVICE	$V_{REVERSE}$	$I_{FORWARD}$	t_{rr}	PACKAGE
SGS8R05- ->20	50V/200V	8 A	35 ns	DO-220
SGS15R05- ->20	50V/200V	15 A	35 ns	DO-220
SGS30R05- ->20	50V/200V	30 A	35 ns	SOD- 93
SGS35R120	1200 V	35 A	100 ns	SOD- 93
SGS45R80	800 V	45 A	100 ns	SOD- 93
SGS60R40	400 V	60 A	100 ns	SOD- 93

The effect of parasitic inductances L_D and L_S and of the diode connections respectively on V_{DS} and I_D are shown in Fig. 24.

Fig. 24 - Shows the effects of the parasitic inductances L_D and L_S and of the diode connections respectively on V_{DS} and I_D waveforms



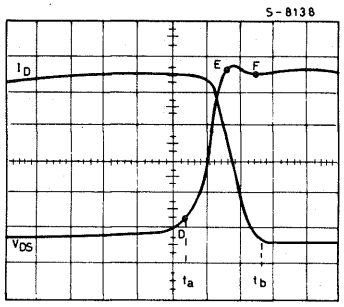
TURN-OFF

The circuit in Fig. 18 is still useful in evaluating the behaviour of an SGS POWER MOS device turning off an inductive load. The initial conditions can be assumed to be:

1) $I_D = I_{LOAD}$
2) $V_{DS} = V_{DS\ (on)} = R_{DS\ (on)} \times I_D$
3) Freewheeling diode reverse biased.

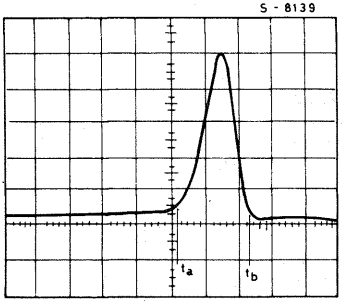
In fig. 25 typical waveforms for V_{DS} and I_D during turn-off phase are represented

Fig. 25 - V_{DS} and I_D during turn-off



t: 50ns/div, V: 40V/div, I: 1.2A/div, Rg=25Ω, Vg=10 V

Fig. 26 - Output Energy during turn-off phase.



t: 50ns/div, P: 200 W/div, E=70.6μJ

It is possible to distinguish two phases:
1) From point D to point E (Fig. 25).
During this phase V_{DS} increases while I_D, the diode being reversed biased, remains constant and equal to I_{LOAD}.
2) From point E to point F (Fig. 26).
During this phase the diode begins conducting allowing the current in the load to flow through itself and I_D of the POWER MOS device to fall. In Fig. 26 the output energy consumption during the turn-off phase is represented.
Also in this case a high cross over between V_{DS} and I_D occurs, even if there is no reverse recovery of the diode as during the turn-on phase. The Miller effect in the SGS POWER MOS device delays the rise of V_{DS} and therefore the switch-on of the freewheeling diode D.

Energy in switching

From the energy point of view there are four distinct phases, each contributing in a different way to the total dissipated energy per cycle. They are:

1) ON - STATE
2) OFF-STATE
3) Transition ON-OFF
4) Transition OFF-ON

The ON-STATE

In the ON-STATE, when the channel is completely open, SGS POWER MOS devices have a minimun $R_{DS\ (ON)}$ which is temperature dependent. The power dissipation at a given instant is obtained from the equation:

$$P_{D(ON\text{-}STATE)} = R_{DS(ON)}(T_j) \times I_D^2$$

$$= R_{DS(ON)} \times [1 + \alpha(T_j - 25°C)] \times I_D^2$$

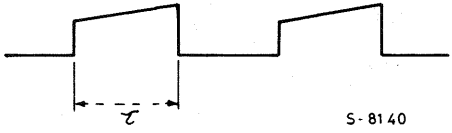
where $\alpha = 8 \times 10^{-3}\ °C^{-1}$, a positive coefficient.

The lower $R_{DS(ON)}$ the lower the power dissipation. The manufacturers can control $R_{DS(ON)}$:

1) by improving the back metalization of the chip and its attachment to the case.
2) by controlling the epitaxial growth of the DRAIN.
3) by optimizing the horizontal lay-out of the Power Mos structure (high cell density).

Fig. 27 - Can be used to calculate the energy consumption during the ON phase

Fig. 27 - I_D waveform during the working cycle



The slope of I_D during the conduction phase is given by $dI_D/dt = V_{DD}/L$ (see Fig. 19).
The lost energy per cycle is given by:

$$E_{on} = \int_0^{\tau} I_D^2(t) \times R_{DS(ON)} \times dt$$

where τ is the pulse width.

In most cases the slope of I_D is quite gentle so if we call I the average I_D between t_1 and t_2, ($t_1 - t_2 = \tau$) in Fig. 27, this energy can be calculated with good approximation as follows:

$$E_{on} = R_{DS(ON)} \times T_j \times I^2 \times \tau$$

In Fig. 28, 29, and 30 the curves of E_{on} are shown for three different devices. Each curve is characterized by different values of τ.

Fig. 28 - On state energy values as a function of the drain current for SGSP301

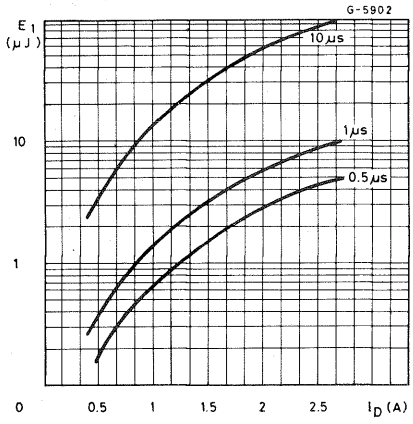


Fig. 29 - On-state energy waveforms as a function of the drain current SGSP575.

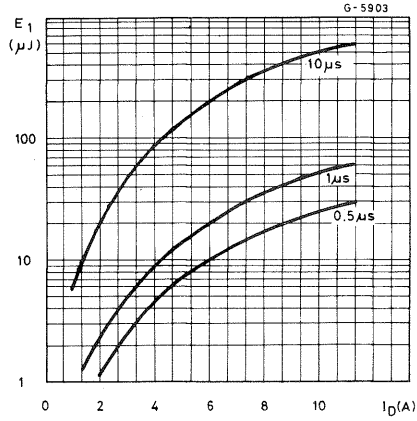
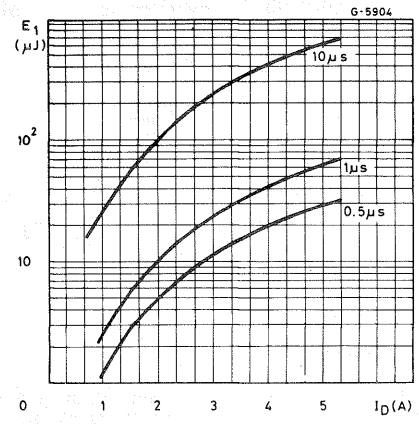


Fig. 30 - On-state energy values a function of the drain current SGSP531



OFF-STATE

When the device is switched off the V_{DS} voltage is equal to V_{DD} (see Fig. 25). Only the leakage current I_{DSS} flows through the device. The energy consumption during this period is given by:

$$E_o = V_{DD} \times I_{DSS} \times t_{off}$$

This energy is in the range of pJ and it is negligible in comparison to that dissipated during the switching and the ON-STATE.

Transitions

During transitions the dissipated power, instant by instant, is:

$$P(t) = V_{DS}(t) \times I_D(t)$$

The power waveform is triangular in shape (see Fig. 20 and Fig. 26). Integrating P(t) the energy consumption per cycle during OFF-ON and ON-OFF transitions can be obtained by:

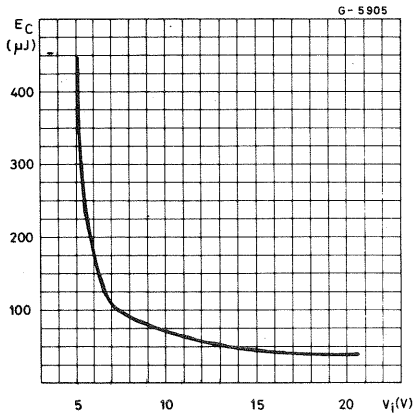
$$E = \int_{t_a}^{t_b} P(t)dt = \int_{t_a}^{t_b} V_{DS}(t)\, I_D(t)dt$$

Where t_a and t_b respectively represent the begining and the end of transitions. These amounts of energy principally depend on the intersecting point between voltage and current, and on the switching speed.
In both transitions the intersecting points are very high and occur at a voltage value close to that of the supply. The intersecting points represent the power to be switched, consequently in order to optimize the energy consumption the time interval $t_a - t_b$ must be reduced by acting on different driving and lay-out parameters (V_{GS}, R_{GS}, parasitic inductances).

Fig. 31 - Shows the energy lost per cycle during

the ON/OFF transition, as a function of V_i for an SGSP369 switching 4A at 200 V.

Fig. 31 - Values of the energy lost per cycle as a function of the gate voltage



Computing the total energy consumption per cycle

The previous analysis allows us to calculate the total energy dissipated per cycle in an SGS POWER MOS device. In fact the total energy can be expressed as:

Eq.3 $E_{TOT} = E_{on}+E_{off}+E_{off/on}+E_{on/off}+E_p$

where:
E_{TOT} = total energy dissipated per cycle
E_{on} = energy dissipated during the on-state
E_{off} = energy dissipated during the off-state
$E_{off/on}$ = energy dissipated during the turn-on
$E_{on/off}$ = energy dissipated during the drive circuit
E_p = total energy dissipated by the drive circuit

Neglecting E_{off} (= pJ) and E_p (= nJ) Eq. 3 can be re-written as:

Eq.4 $E_{TOT} = E_{on} + E_{off/on} + E_{on/off}$

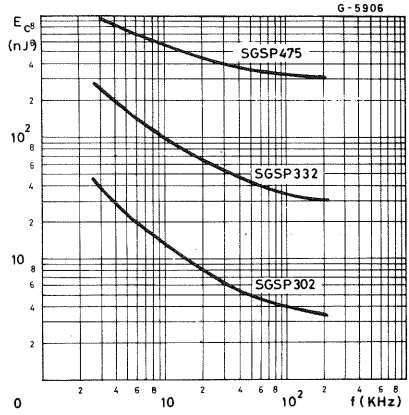
These three terms in Eq. 4 depend in differing amounts on the operating conditions of the device I_D, V_{DD} and the duty cycle.
To give some idea of the total energy dissipated per switching cycle the following operating conditions have been fixed and the results of energy measurements made shown in Fig. 32.

V_{DD} = 1/2 BV_{DSS} of the device under test

I_D = 3/4 I_{DMAX} of the device under test

duty cycle = 50%

Fig. 32 - Total energy lost per cycle as a function of the frequency with a fixed duty eycle of 50%



The curves tend towards a horizontal asyntote that represents the cross-over energy (turn-on + turn-off, which is frequency independent).
It is clear that the effect of E_{on} is of great importance at low frequencies, and the higher the $R_{DS(ON)}$ the greatest the effect.

HIGH VOLTAGE TRANSISTORS WITH POWER MOS EMITTER SWITCHING

INTRODUCTION

This paper summarizes the results of an investigation carried out on power devices with both MOS and BIPOLAR parts working together in the same circuit. The "emitter drive" configuration was considered, with switching power supply applications in mind.

The devices used are:

Power MOS:	SGSP321, SGSP352
Bipolar transistors:	BUV48, BU508A
Ultrafast bipolar transistors: (Hollow Emitter)	SGSD00035, SGSD00039
Fast darlingtons:	SGSD00031, BU810

In the case of flyback switching power supplies a practical example is also described.

CIRCUIT DESCRIPTION

The term "emitter switching" describes a circuit configuration where a low voltage transistor (MOS or Bipolar) switches off the emitter current of a high voltage transistor, and consequently the transistor itself.

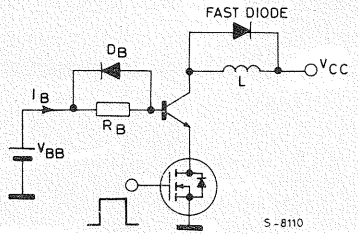
This configuration combines the fast switching of a low voltage device with the high power switching of a high voltage device, since:

high current x high voltage = high power switching.

The combination of a high voltage bipolar and a low voltage Power MOS is preferable due to the high switching speed and the low driving energy of the combined power switch.

The base of the high voltage bipolar device is driven by a constant voltage source. The energy dissipated to drive the high voltage bipolar device depends on the losses that the forward bias current I_{B1} generates in the resistance in series with R_B, $I_{B1}^2 \cdot R_B \cdot t$. This power dissipation can only be reduced by using high gain transistors of darlingtons. (See Fig. 1)

Fig. 1 - The basic circuit used for the evaluation of the emitter switching system. The base drive circuit used is shown for comparison



The diode in series with the base serves to clamp the base overvoltage at turn-off.

The two transistor stage is driven by the gate of the low voltage Power MOS. Very low driving energies, about 180nJ per cycle, are involved in the charging and discharging of the input capacitances.

Consequently the stage can be directly driven by the output of suitable linear integrated circuits.

The possibility of direct driving by an IC output together with the excellent switching speed make this configuration extremely suitable for switching power supplies at frequencies of 50KHz or even higher.

CIRCUIT OPERATION

As we have seen, the forward base current I_{B1} is fixed by the external circuitry:

$$I_{B1} = \frac{V_{BB} - V_{BEsat} - V_{DSon}}{R_B}$$

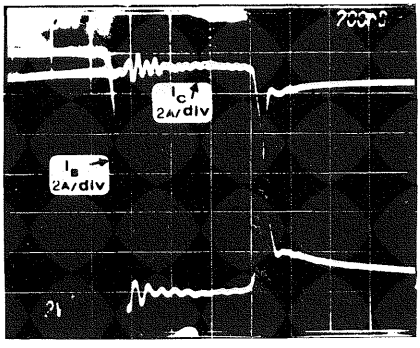
The collector current instead depends on the load, and in general, varies with the time.

The turn-on and turn-off phases can be analyzed separately.

TURN-OFF

When the driving signal to the Power MOS is low the drain current is interrupted and the emitter current of the high voltage bipolar falls to zero. The emitter reaches the base voltage and won't carry any more current. As a result the collector current can only flow through the base, becoming a reverse base current that depletes the base to collector junction. This reverse base current I_{B2}, from the moment when the emitter current disappears, coincides with the collector current. See photo 1. The stored charge is removed in a typically very violent, and consequently rapid manner.

Photo 1 - Base and collector current at turn-off



As a result the storage time is substabtially reduced. The fall time, which is related to the recombination under the emitter, is also generally reduced.

Typical values for the fall and storage time of the SGS devices used in the test are shown in Table 1, for both emitter and the base drive circuits.

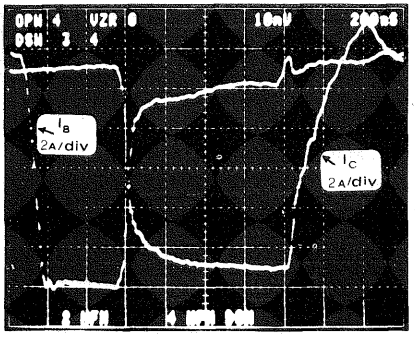
Table 1 - Typical tf and ts on inductive load

Device	IC(A)	EMITTER SWITCHING		BASE SWITCHING	
		tstorage	tfall	tstorage	tfall
BUX48	10	500ns	100ns	2μs	200ns
BU508A	5	800ns	300ns	6μs	400ns
SGSD00031	10	400ns	100ns	1.2μs	100ns
BU810	5	300ns	150ns	800ns	150ns
SGSD00035	10	300ns	50ns	800ns	50ns
SGSD00039	5	300ns	40ns	700ns	50ns

TURN-ON

When the Power MOS is in the ON state, the bipolar device also starts conducting. The dynamic behaviour (See Photo 2) does not differ in any substantial way from the usual case of the base drive.

Photo 2 - Base and collector current at turn-on



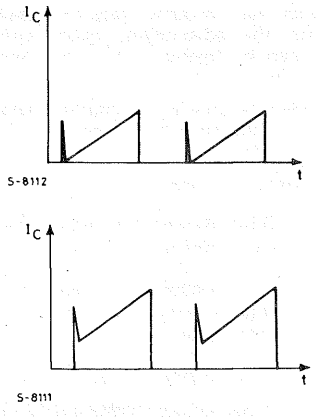
The dynamic saturation transient $V_{CEsat\,dyn}$ is also practically the same with a base drive as with an emitter drive. The collector current, when the collector load is the primary winding of a switching transformer, can vary according to two possibilities. (See Fig. 2)

a) After the initial peak due to the recovery of the diode present on the secondary winding, the collector current increases linearly starting from zero

b) After the same initial peak, the collector cur-

rent increases linearly starting from the value memorized in the magnetic circuit at the end of the previous cycle.

Fig. 2 - Collector current waveforms with varying load



REVERSE BIAS SAFE OPERATING AREA

A problem that occurs in bipolar transistors is damage caused by "current crowding".

Fig. 3a illustrates current flowing in a typical bipolar device. Fig. 3b shows how, when the device is turned off and the current begins to die away, the current focuses with a high concentration under the emitter. This high current density can damage or destroy the transistor.

Fig. 3a

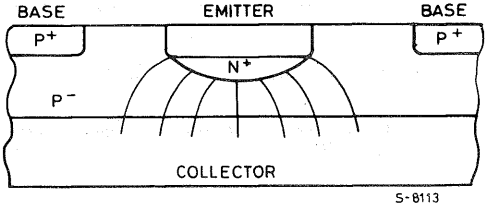
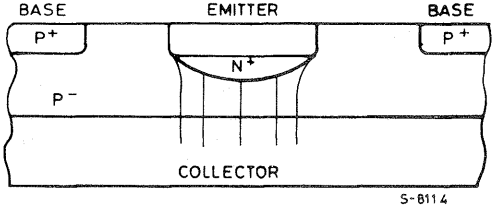


Fig. 3b -



The energy dissipated within a bipolar power transistor at turn-off can be found graphically from a plot of I_C versus V_{CE} at turn-off. Three cases are shown in Figures 4a, b and c. The shaded area is proportional to the energy that is dissipated in the device during turn-off.

Fig. 4a - Slow turn-off. No crowding but high average heating

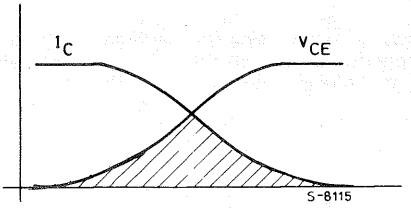


Fig. 4b - Fast turn-off. Crowding with low average heating but possible high peak power

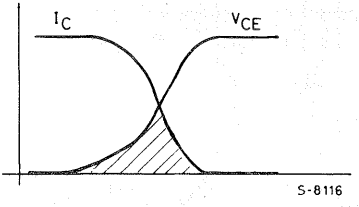
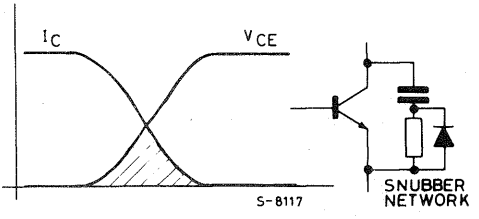


Fig. 4c - Fast turn-off (with V_{CE} delayed by snubber network)



Consequently turn-off times affect the SOA of the device, (Fig. 5b). These problems can be overcome using emitter switching.

The way the stored charge is swept away in the high voltage bipolar device when it is driven by the emitter, produces some interesting consequences.

The stored charges are evacuated through the base contact when the emitter current is zeroed and not later than a few tens of ns after the beginning of the storage interval. Consequently, during the turn-off, no charge is injected from the emitter into the base. Although the reverse base current is quite relevant, no focusing of the current in the centre of the emitter fingers takes place.

The bipolar device therefore exhibits an energy absorbing ability at the turn-off RBSOA that is substantially higher than if a normal base drive were used. With a base drive the emitter would inject charges and the voltage drop across the distributed base resistence would induce the "emitter crowding" phenomenon.

The practical evidence for all the transistors investigated (BUV48, BU508A, SGSD00035, SGSD00039) shows that the reverse bias safe operating area (RBSOA) extends right up to the BV_{CES}! (See fig. 5)

This extreme effect is unfortunately much less pronunced when using fast darlingtons. The higher complexity of the charge extraction mechanism and the charge injection from the emitter into the base in the driver transistor imply that the RBSOA extension is almost irrelevant.

Fig. 5a - Reverse bias safe operating area

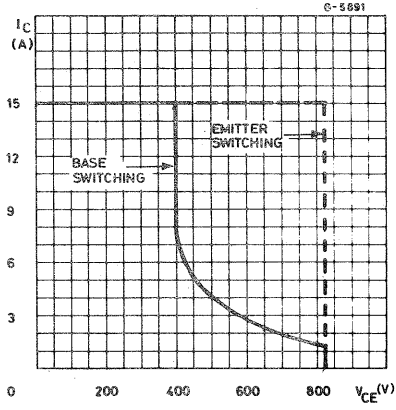
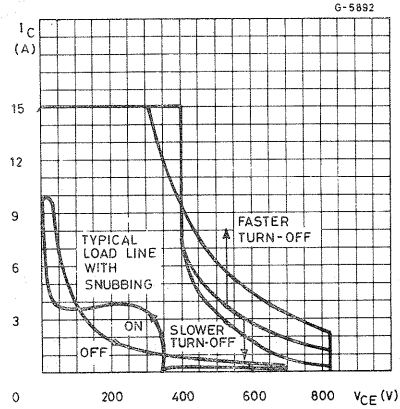


Fig. 5b - How reverse bias safe operating area changes for:
i) slow turn-off
ii) fast turn-off



A POSSIBLE APPLICATION

A possible application of the "emitter switching" configuration is shown in Figure 6, where a switching power supply operating in a "flyback" mode has been implemented.

The basic criteria used in choosing the values of the circuit elements are given below. The purpose of the study was to demostrate the feasibility and to evaluate the advantages. Exact circuit element values can be further optimized, especially in the case of the transformer.

The power source is the mains singlephase, 220V a.c.), and the switching frequency can be set to 50KHz or more.

The devices used were:

Q1: Fast darlingtons with $BV_{CES} \geqslant 600V$ for 110V line
- SGS BU810 for current up to 5A
- SGSD00031 for current above 5A

Fast transistor with $BV_{CES} \geqslant 800V$ for 220V line
- SGSD00039 for currents up to 5A
- SGSD00035 for currents up to 10A

Q2: Low voltage POWER MOS (BV_{DSS}=50V)
- SGSP352 for currents up to 5A
- SGSP322 for currents above 5A

Q3: High voltage, low current POWER MOS ($BV_{DSS} < = 400V$)
- SGSP354

Control IC: SGS UC3842

DZ2: Zener diode 2W/20V

D1: 25V diode, with I_C peak rating as high as 10A for 500ns

C6: Electrolytic capacitor, 1000μF, 25V. It absorbs possible variations of V_{BB}.

R3: Resistor setting the forward bias base current of the darlington:

$$R3 = \frac{V_{CE} - V_{BE\,sat} - V_{DSon} - R7\,I_D}{I_{B1}}$$

Its power rating must exceed $R3 \cdot I_B^2 \cdot t$ (in practice 3W)

R7: Shunt resistor to sense the switch current. The over current I_{Smax} protection is set according to

$$R7 = \frac{1V}{I_{Smax}} -$$

C4, R6: RC network, filtering the disturbances induced by the switching transients on the I_{Smax} protection input.

C3, R5: RC network, setting the switching frequency and the maximum duty cycle, according to the UC3842 data sheet.

$t_{charge} = 0.55\ R_5\ C_3$
$t_{discharge} = R_5 \times C_3\ \ell n\ [(6.3\ R_5 - 2.7)/6.3\ R_5\text{-}4)]$
$f = 1/(t_c + t_d)$

R8, R9: Resistive divider, of the feedback voltage, from a secondary sense winding, rectified by D5 and C5. The divided voltage is compared by the control IC to an interval reference of 2.5V.

C2, R4: Compensating network in the error amplifier of the feed-back voltage.

R1: Resistor biasing the Q3 gate (1.2MΩ, 1/4W)

R2: Resistor that limits the inrush current through the POWER MOS Q3 at the turn-on (1.2KΩ, 2W)

D4: Fast recovery diode
Its voltage/current ratings depend on the particular secondary winding it rectifies.

D5: Low current/low voltage diode

D3, R10, C8: Snubber network (Fig. 6 shows just one of the possible configurations).

$$C8 = \frac{L_d\ I_c^2}{V_{os}^2}$$

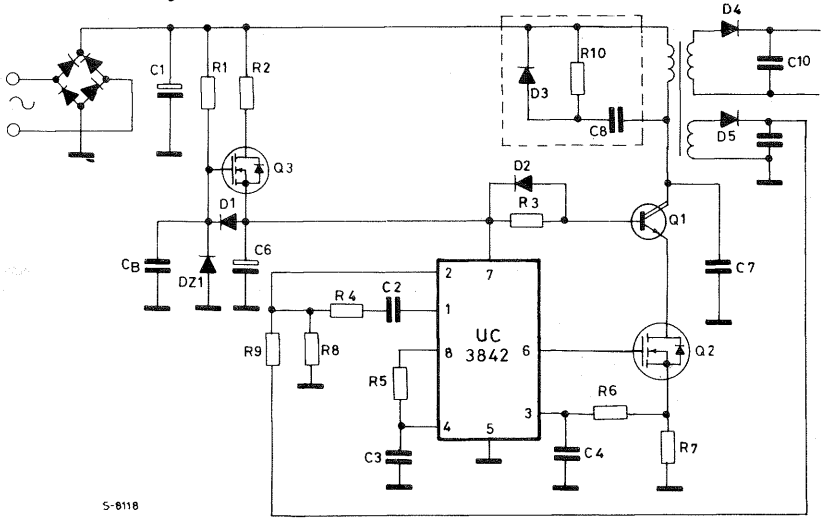
$R10 = 1/4fC8$
$P\ (R_{10}) = 1/2\ L_d\ I_d^2 f$

where:

f = switching frequency
L_d = stray inductance of the transformer
V_{os} = maximum voltage overshoot admitted
D_3: is a 400V fast recovery diode
C_7: Possible capacitor reduces the cross-over of the Darlington (3 to 6nF)

It is important to note that, the power transistor Q3 acts only at the turn-on of the power supply and when the capacitor C6 supplies more energy to the base of the darlington and to the supply input of the IC than is returned to C6 during the turn-off of the darlington, Q1.

Fig. 6 - "Emitter switching" circuit



CONCLUSION

The "emitter drive" configuration exhibits some clear differences with respect to the usual "base drive" configuration, and they can be particularly useful in switching power supply applications:

- Substantial reduction of the storage time and improvement of the fall time

Switching frequencies of 50KHz and higher are possible

- The dynamic drive circuitry is simplified. The negative voltage supply is not required to remove the stored charge from the base. The energy needed to drive the gate of the POWER MOS is very low (180nJ per cycle).
- Extremely high ruggedness at the turn-off of the inductive load (i.e. very large RBSOA) if the high voltage bipolar part is a transistor.
- Higher power dissipation in the on-stage, due to the additional losses in the POWER MOS ($I_D^2\ R_{DSon}\ ton$)

This last point is the only disadvantage, but it is more than compensated for if switching at high frequencies. The lower switching losses (a saving each cycle) can justify the higher on-state losses (a fixed expenditure) as soon as the switching frequency is high enough, which is often the case in switching power supplies.

PRODUCT SELECTOR

HIGH CURRENT SWITCHING REGULATORS

PARAMETERS	DEVICES			
	L296	L4960	L4962	L4964
Voltage Reference (%)	± 2	± 4	± 4	± 3
Output Voltage Range	V_{REF} to 40V	V_{REF} to 40V	V_{REF} to 40V	V_{REF} to 28V
Output Current (A)	4.0	2.5	1.5	4.0
Internal Current Limiting	●	●	●	●
Soft Start	●	●	●	●
Inhibit Input	●			●
Reset Output	●			●
Crowbar Control	●			
Max. Oscillator Frequency (KHz)	200	120	120	120
Separate Oscillator Synch.	●			●
Thermal Protection	●	●	●	●
Package	Multiwatt 15	Heptawatt	12 + 2 + 2	Multiwatt 15

PWM CONTROLLERS

PARAMETERS	OPERATING TEMPERATURE: 0 to 70°C							
	SG3524	UC3524A	SG3525A	SG3527A	UC3840	UC3842	UC3846	UC3847
Voltage Reference (%)	± 8	± 2	± 2	± 2	± 2	± 2	± 2	± 2
Soft Start			●	●	●		●	●
PWM Latch		●	●	●	●	●	●	●
Under Voltage Lockout		●	●	●	●	●	●	●
Pulse by Pulse Current Limiting		●			●	●	●	●
Shutdown Terminal	●	●	●	●	●	●	●	●
Output Current (A)	0.1	0.2	0.1 (0.4)	0.1 (0.4)	0.2	0.2 (1)	0.2	0.2
Feedforward					●	●	●	●
Max. Oscillator Frequency (KHz)	300	500	500	500	500	500	500	500
Dual Uncommitted Outputs	●	●						
Single Ended Output					●	●		
Totem Pole Outputs			●	●			●	●
Separate Oscillator Synch. Terminal			●	●			●	●
Adjustable Deadtime Control			●	●	●	●	●	●
Latch Off or Continuous Retry Mode					●		●	●
Double Pulse Suppression		●					●	●
Low Current Start-Up					●	●		
Package	DIP-16				DIP-18	Minidip	DIP-16	

PWM CONTROLLERS

PARAMETERS	OPERATING TEMPERATURE: -25 to 85°C							
	SG2524	UC2524A	SG2525A	SG2527A	UC2840	UC2842	UC2846	UC2847
Voltage Reference (%)	± 4	± 1	± 1	± 1	± 1	± 1	± 1	± 1
Soft Start			●	●	●		●	●
PWM Latch		●	●	●	●	●	●	●
Under Voltage Lockout		●	●	●	●	●	●	●
Pulse by Pulse Current Limiting		●			●	●	●	●
Shutdown Terminal	●	●	●	●	●		●	●
Output Current (A)	0.1	0.2	0.1 (0.4)	0.1 (0.4)	0.2	0.2 (1)	0.2	0.2
Feedforward					●	●	●	●
Max. Oscillator Frequency (KHz)	300	500	500	500	500	500	500	500
Dual Uncommitted Outputs	●	●						
Single Ended Output					●	●		
Totem Pole Outputs			●	●			●	●
Separate Oscillator Synch. Terminal			●	●			●	●
Adjustable Deadtime Control			●	●	●	●	●	●
Latch Off or Continuous Retry Mode					●		●	●
Double Pulse Suppression		●					●	●
Low Current Start-Up					●	●		
Package	DIP-16				DIP-18	Minidip	DIP-16	

PWM CONTROLLERS

PARAMETERS	OPERATING TEMPERATURE: -55 to 125°C							
	SG1524	UC1524A	SG1525A	SG1527A	UC1840	UC1842	UC1846	UC1847
Voltage Reference (%)	± 4	± 1	± 1	± 1	± 1	± 1	± 1	± 1
Soft Start			●	●	●		●	●
PWM Latch		●	●	●	●	●	●	●
Under Voltage Lockout		●	●	●	●	●	●	●
Pulse by Pulse Current Limiting		●			●	●	●	●
Shutdown Terminal	●	●	●	●	●		●	●
Output Current (A)	0.1	0.2	0.1 (0.4)	0.1 (0.4)	0.2	0.2 (1)	0.2	0.2
Feedforward					●	●	●	●
Max. Oscillator Frequency (KHz)	300	500	500	500	500	500	500	500
Dual Uncommitted Outputs	●	●						
Single Ended Output					●	●		
Totem Pole Outputs			●	●			●	●
Separate Oscillator Synch. Terminal			●	●			●	●
Adjustable Deadtime Control			●	●	●	●	●	●
Latch Off or Continuous Retry Mode					●		●	●
Double Pulse Suppression		●					●	●
Low Current Start-Up					●	●		
Package	DIP-16				DIP-18	Minidip	DIP-16	

LOW DROP VOLTAGE REGULATORS

Type	Low drop	Very low drop	Transient protection				Reset	Short circuit protection	Reverse voltage protection	Output voltage			
			± 100	± 80	± 60	± 40				5V	8.5V	10V	12V
L387		●					●	●	●	●			
L487		●		●			●	●	●	●			
L2605	●		●					●	●	●			
L2685	●		●					●	●		●		
L2610	●		●					●	●			●	
L4705		●		●				●	●	●			
L4785		●		●				●	●		●		
L4710		●		●				●	●			●	
L4805		●			●			●	●	●			
L4885		●			●			●	●		●		
L4810		●			●			●	●			●	
L4812		●			●			●	●				●
L4920		●			●			●	●	adjustable			
L4921		●			●			●	●				
L4940		●				●		●	●	●			
LM2930A		●				●		●	●	●			
LM2931A		●			●			●	●	●			
LM2935 (*)		●			●		●	●	●	●			

PROPRIETARY VOLTAGE REGULATORS

I_o max (A)	Type	Regulated output voltage (V)						Package
			5	8.5	10	12		
4	L296 (**)	5.1V ← adjustable → 40V						Multiwatt 15
	L4964 (**)	5.1V ← adjustable → 28V						
2.5	L4960 (**)	5V ← adjustable → 40V						Heptawatt
2	L200CH/CV L200CT/T	2.9V ← adjustable → 36V						Pentawatt TO-3 (4 lead)
1.5	L4962 (**)	5V ← adjustable → 40V						Powerdip 12 + 2 + 2
	L4940		●					TO-220
0.5	L387		●					Pentawatt
	L487		●					Pentawatt
	L2600V		●	●	●			TO-220
	L4700CV		●	●	●			TO-220
	L4800CV		●	●	●	●		TO-220
	L4800CX		●	●	●	●		SOT-82
	L4901 (*)		●					Heptawatt
	L4902 (*)		●					Heptawatt
	L4916			●				Minidip
	L4920	1.25V ← adjustable → 20V						Pentawatt
	L4921							Minidip

(*) Dual regulator (**) Switch-mode

STANDARD POSITIVE VOLTAGE REGULATORS

I_O max (A)	Type	Regulated output voltage (V)												Package
			5	6	7.5	8	9	10	12	15	18	20	24	
2 (*)	L78S00CV		●		●		●	●	●	●	●		●	TO-220
	L78S00CT/T		●		●		●	●	●	●	●		●	TO-3
1.5	LM117K	1.2V ⟵ adjustable ⟶ 37V												TO-3
	LM217K													TO-3
	LM317K													TO-3
	LM317T													TO-220
1	L7800CV		●	●		●			●	●	●	●	●	TO-220
	L7800ACV (**)		●	●		●			●	●	●	●	●	TO-220
	L7800CT/T		●	●		●			●	●	●	●	●	TO-3
0.5	L78M00CV		●	●		●			●	●	●	●	●	TO-220
	L78M00CX		●	●		●			●	●	●	●	●	SOT-82
0.15	LM723CD	2V ⟵ adjustable ⟶ 36V												SO-14
	LM723CH													TO-100
	LM723CJ													DIP-14C
	LM723CN													DIP-14P
	LM723J													DIP-14C
	LM723H													TO-100

STANDARD NEGATIVE VOLTAGE REGULATORS

I_O max (A)	Type	Regulated output voltage (V)									Package
			-5	-5.2	-8	-12	-15	-18	-20	-24	
1	L7900ACV (**)		●	●	●	●	●	●	●	●	TO-220
	L7900CV		●	●	●	●	●	●	●	●	TO-220
	L7900CT/T		●	●	●	●	●	●	●	●	TO-3

(*) Proprietary SGS selection (**) Output voltage = ± 2%

SWITCHING REGULATOR CONTROLLERS FOR TV AND MONITORS

TYPE	DESCRIPTION	PACKAGE
TDA4601	Designed to regulate and control the high voltage transistor of a switching power supply. – $V_{S\,MAX}$ = 20V - $I_{S\,MAX}$ = 160mA – Operating frequency: 10 to 80KHz.	DIP-18 (9 + 9)
TDA8130	Provides the necessary features to implement off-line, fixed frequency current mode control schemes. Protection circuitry includes built-in voltage lockout, pulse by pulse limiting and an antimagnetization circuit.	Minidip
TDA8132	Provides the same features and functions of the TDA8130, but with added: – Enable input – Over and under voltage detectors – Overload identification – Synch. facility.	DIP-14

SPECIAL FUNCTIONS

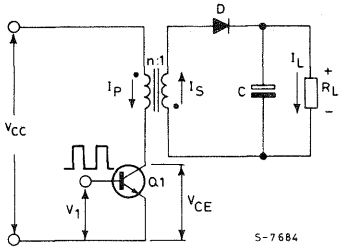
TYPE	DESCRIPTION	PACKAGE
TL7700 series	Supply voltage supervisors designed for use as reset controllers in μP systems. During power-up the device tests the supply voltage and keeps the reset outputs active as long as the supply voltage has non reached its nominal voltage value. – V_S = 3V to 18V – Temperature compensated voltage reference – Externally adjustable pulse width	Minidip
UC2906 UC3906	Battery charger controllers designed to optimally control the charge and hold cycle for sealed lead acid batteries. The output driver will supply 25mA Max to an external pass device.	DIP-16

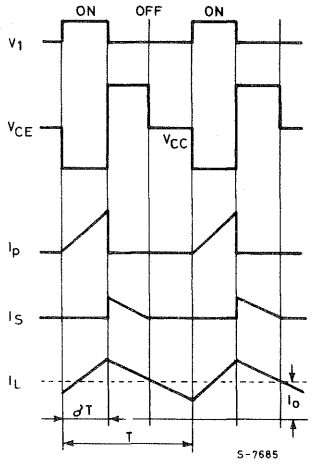
SWITCHING REGULATOR MODULES

TYPE	Input Voltage V	Output Voltage V	Output Current A	Current Limit A	Line Regulation dB	Load Regulation mV/A	Temp. Stability mV/°C	Crowbar Intervention V	Output Noise mV	Efficiency
GS-R405	8-48	5	4	5	60	20	0.2	6	25	75
GS-R405S	8-48	5	4	5	60	20	0.2	6	25	75
GS-R412	15-48	12	4	5	60	40	0.5	15	30	85
GS-R415	18-48	15	4	5	60	60	0.6	18	40	90
GS-R424	27-48	24	4	5	60	90	1	29	50	90
GS-R400V	V_o+3-48	5-40 ADJUST	4	5	60	20/90	0.2/1.6	1.2 V_o	25/50	75/90

PIN	FUNCTION
INH	**Inhibit.** TTL compatible input. When high, module is disabled. Connect to ground if not used.
RT	**Reset Output.** On GS-R405S only. RT is high (5V) 100 ms after output voltage reaches nominal value (5V).
V_I	**Input.** Unregulated DC input. Maximum voltage must not exceed 48V.
GND_1	**Ground.** Common ground for input voltage.
GND_2	**Ground.** Common ground of high current path. Case of module must be isolated from ground.
S^-	**Sensing negative.** Senses the actual ground of a remote load.
S^+	**Sensing positive.** Senses voltages on a remote load.
V_o	**Output.** Regulated and stabilized DC voltage. Max output current is 4A. Protected against short circuit to ground or to supply.
P	**Output voltage regulation.** On GS-R400V only. A variable resistor (18KΩ max) connected between this pin and S^+ can adjust the output voltage.

OFF LINE SWITCHING POWER SUPPLIES
FLYBACK CONFIGURATION





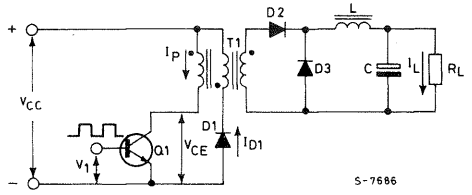
ADVANTAGES:

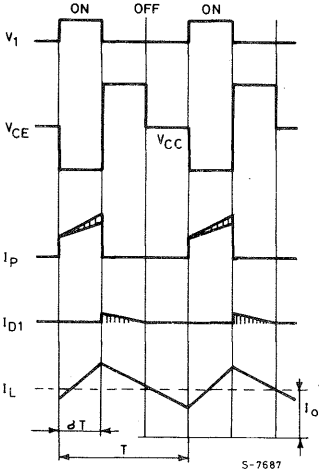
- SIMPLE TRANSFORMER
- NO HIGH VOLTAGE FAST DIODES
- ONLY ONE SECONDARY DIODE
- SIMPLE FILTER

DISVANTAGES:

- $V_{CE\,(max)} = 2 \times V_{CC} + V_S$ (n2/n1)
- HIGH RATIO $I_{C\,(pk)}/I_{C\,(av)}$
- MOST STRESS ON POWER TRANSISTOR FOR GIVEN OUTPUT POWER

OFF LINE SWITCHING POWER SUPPLIES
SINGLE TRANSISTOR FORWARD CONFIGURATION





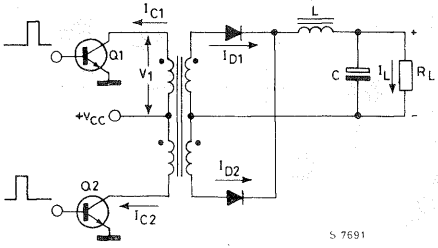
ADVANTAGES:

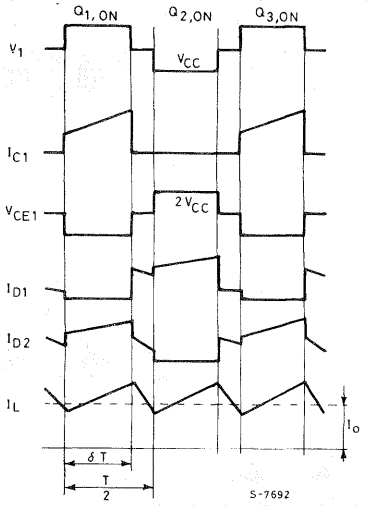
- ONLY ONE HIGH VOLTAGE FAST DIODE
- MORE USEFUL CURRENT WAVEFORM (LOWER RATIO $I_{C\,(pk)}/I_{C\,(av)}$)

DISVANTAGES:

- $V_{CE\,(max)} = 2 \times V_{CC}$
- COMPLEX TRANSFORMER

OFF LINE SWITCHING POWER SUPPLIES
PUSH-PULL CONFIGURATION





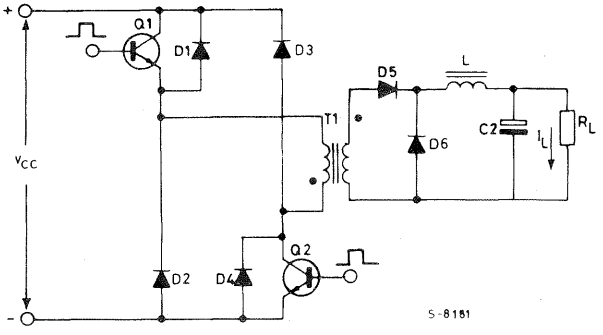
ADVANTAGES:

- BOTH TRANSISTORS ARE DRIVEN WITH RESPECT TO GROUND

DISVANTAGES:

- $V_{CE\ (max)} = 2 \times V_{CC}$
- RISK OF TRANSFORMER CORE SATURATION IF CURRENTS UNBALANCED

OFF LINE SWITCHING POWER SUPPLIES
HALF BRIDGE CONFIGURATION



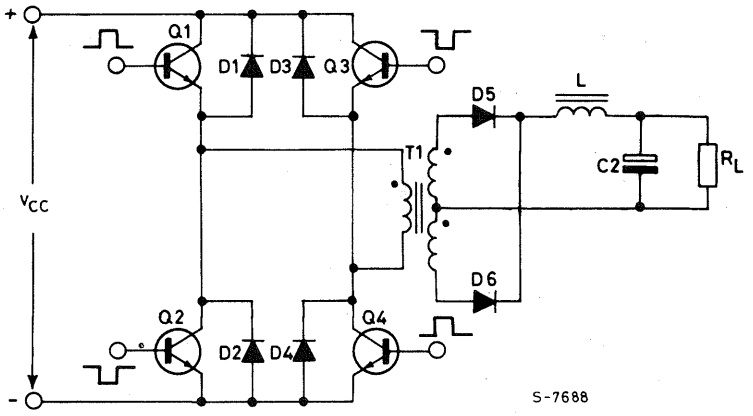
ADVANTAGES:

- SIMPLE TRANSFORMER
- $V_{CE\ (max)} = V_{CC}$

DISVANTAGES:

- Q1 REQUIRES FLOATING DRIVE
- REQUIRES 4 FAST DIODES

OFF LINE SWITCHING POWER SUPPLIES
FULL BRIDGE CONFIGURATION



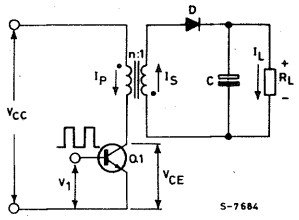
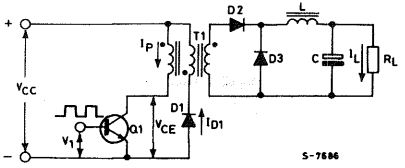
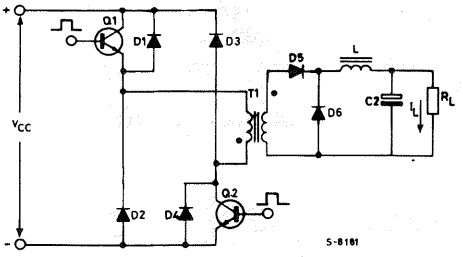
ADVANTAGES:

- SIMPLE TRANSFORMER
- HIGHEST USEFUL POWER PER TRANSISTOR
- $V_{CE\ (max)} = V_{CC}$

DISVANTAGES:

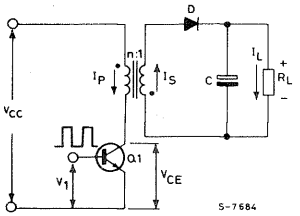
- COMPLEX DRIVE CIRCUITS
- REQUIRES 4 TRANSISTORS AND 4 HIGH VOLTAGE FAST DIODES

20 - 50W CONVERTERS

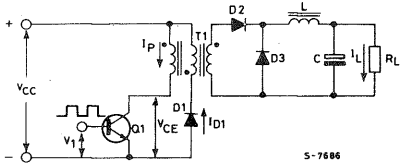
		
FLYBACK	**FORWARD**	**HALF BRIDGE**
20-30kHz	Multiepitaxial Mesa Transistors	Fast Darlingtons
BUX85	**BUX84**	**BU801**
30-75kHz	FASTSWITCH™ Hollow Emitter Transistors	
SGSD00044	**SGSD00044**	**SGSD00042**
> 75kHz	Emitter Switched	POWER MOS
SGSD00044 + SGSP302	**SGSD00042 + SGSP302**	**SGSP239 / SGSP339**

Line = 220V or 110V with voltage doubler

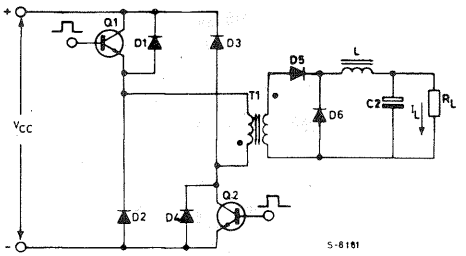
50 - 80W CONVERTERS



FLYBACK



FORWARD

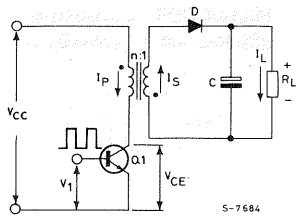
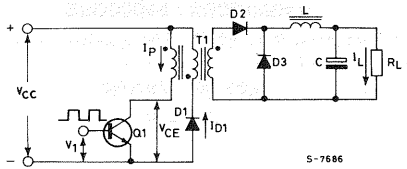
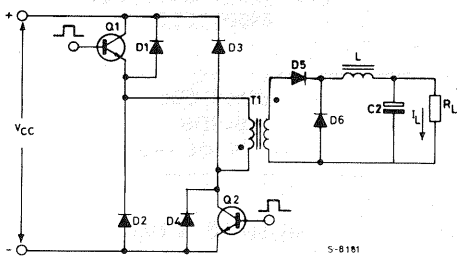


HALF BRIDGE

20-30kHz	Multiepitaxial Mesa Transistors		Fast Darlingtons
	BUT11A	**BUX84**	**BU801**
	BUW11A	**BUT11**	**BU810**
30-75kHz	FASTSWITCH™ Hollow Emitter Transistors		
	SGSD00044	**SGSD00044**	**SGSD00042**
> 75kHz	Emitter Switched		POWER MOS
	SGSD00044 + SGSP352	**SGSD00042 + SGSP302**	**SGS219 / SGSP319**

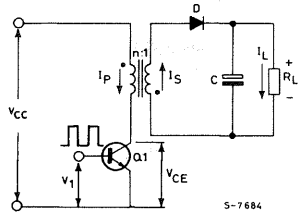
Line = 220V or 110V with voltage doubler

80 - 120W CONVERTERS

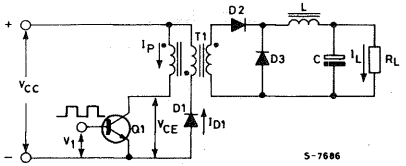
FLYBACK	FORWARD	HALF BRIDGE
		
20-30kHz **BUW12A** **BUV47A / BUX47A**	Multiepitaxial Mesa Transistors **BUT11 / BUW11** **BUV47 / BUX47**	Fast Darlingtons **BU810**
30-75kHz **SGSD00041** **SGSD00039 / SGSD00038**	FASTSWITCH™ Hollow Emitter Transistors **SGSD00044 / SGSD00041** **SGSD00039**	**SGSD00042**
> 75kHz **SGSD00039 + SGSP312**	Emitter Switched **SGSD00041 + SGSP352**	POWER MOS **SGSP369 / SGSP469**

Line = 220V or 110V with voltage doubler

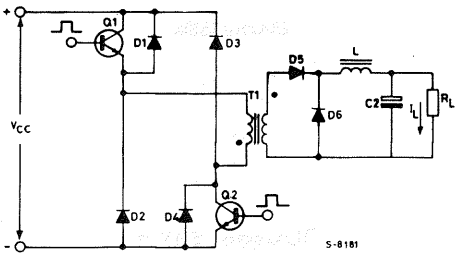
120 - 180W CONVERTERS



FLYBACK



FORWARD

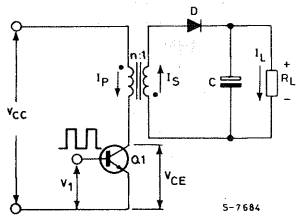


HALF BRIDGE

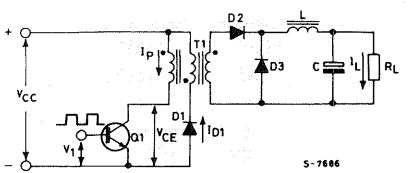
20-30kHz	Multiepitaxial Mesa Transistors		Fast Darlingtons
	BUW12A	**BUW12**	**BU810**
	BUV47A / BUX47A	**BUV47 / BUX47**	**SGS10005P**
30-75kHz	FASTSWITCH™ Hollow Emitter Transistors		
	SGSD00039 / SGSD00038	**SGSD00044 / SGSD00041**	**SGSD00042**
	SGSD00035 / SGSD00034	**SGSD00039 / SGSD00038**	**SGSD00040 / SGSD00037**
> 75kHz	Emitter Switched		POWER MOS
	SGSD00039 + SGSP312	**SGSD00041 + SGSP352**	**SGSP369 / SGSP469**

Line = 220V or 110V with voltage doubler

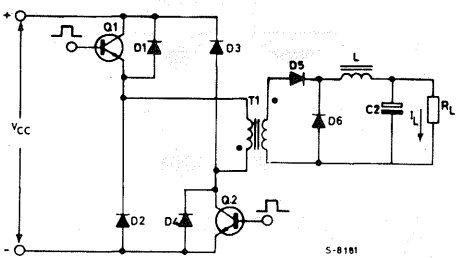
180 - 250W CONVERTERS



FLYBACK



FORWARD

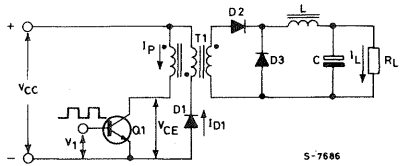


HALF BRIDGE

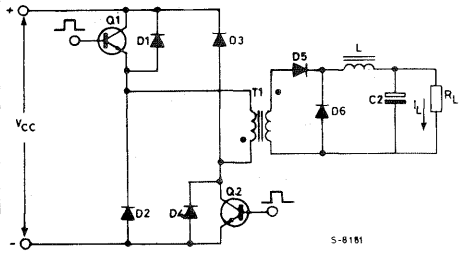
20-30kHz	Multiepitaxial Mesa Transistors		Fast Darlingtons
	BUW13A **BUV48A / BUX48A**	**BUW12** **BUV47 / BUX47**	**SGS10005P**
30-75kHz	FASTSWITCH™ Hollow Emitter Transistors		
	SGSD00035 / SGSD00034	**SGSD00039 / SGSD00038**	**SGSD00040** **SGSD00037 / SGSD00036**
> 75kHz	Emitter Switched		POWER MOS
	SGSD00035 + SGSP362	**SGSD00039 + SGSP312**	**SGSP479 / SGSP579**

Line = 220V or 110V with voltage doubler

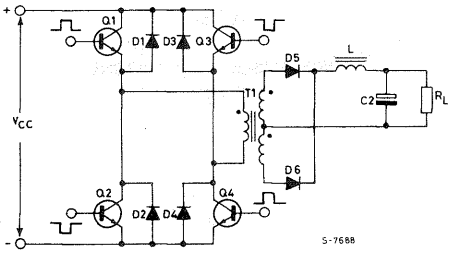
250 - 350W CONVERTERS



FORWARD



HALF BRIDGE

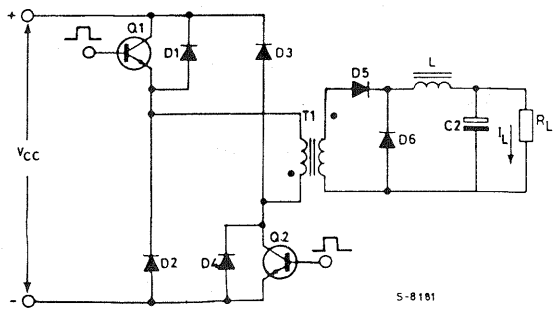


FULL BRIDGE

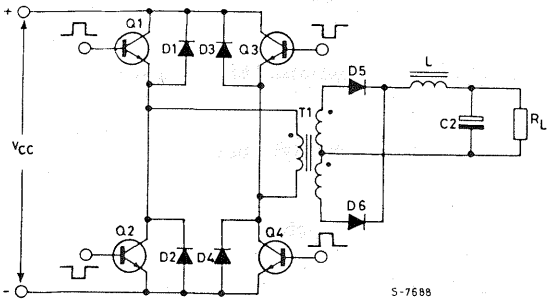
20-30kHz	Transistors **BUW13** **BUV48 / BUX48**	Fast Darlingtons **SGS10005P** **SGSD00030**	**SGS10005P**
30-75kHz	**SGSD00035 / SGSD00034**	FASTSWITCH™ Hollow Emitter Transistors **SGSD00039 / SGSD00038**	**SGSD00037 / SGSD00036**
> 75kHz	Emitter Switched **SGSD00035 + SGSP362**	POWER MOS **SGSP479 / SGSP579**	**SGSP369 / SGSP469**

Line = 220V or 110V with voltage doubler

350 - 700W CONVERTERS



HALF BRIDGE

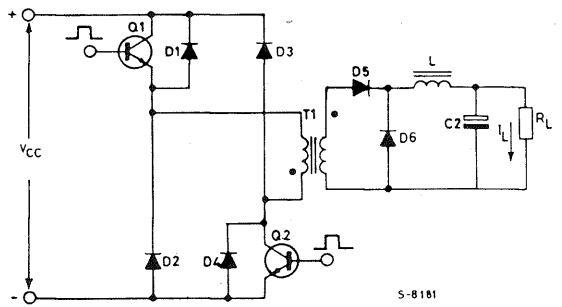


FULL BRIDGE

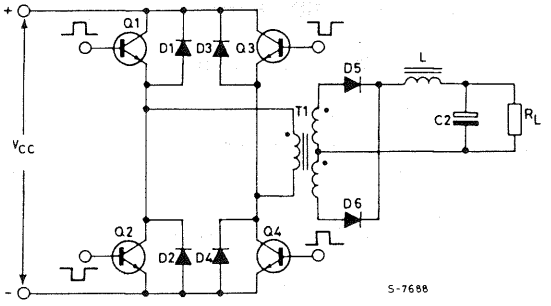
20-30kHz	Fast Darlingtons	
	SGSD00030	**SGS10005P**
20-30kHz	Multiepitaxial Mesa Transistors	
	BUV48 / BUX48	**BUV47 / BUX47**
30-75kHz	FASTSWITCH™ Hollow Emitter Transistors	
	SGSD00033 / SGSD00032	**SGSD00037 / SGSD00036**
> 75kHz	Emitter Switched	POWER MOS
	SGSD00033 + SGSP362	**SGSP479 / SGSP579**

Line = 220V or 110V with voltage doubler

700 - 1200W CONVERTERS



HALF BRIDGE



FULL BRIDGE

20-30kHz	Fast Darlingtons	
SGSD00031 (X2) / **SGS30DB045D** (X1)		**SGS10005P / SGSD00030**
20-30kHz	Multiepitaxial Mesa Transistors	
BUX98 / BUX48		**BUV48 / BUX48**
30-75kHz	FASTSWITCH™ Hollow Emitter Transistors	
SGSD00032		**SGSD00033 / SGSD00032**
> 75kHz	Emitter Switched	
SGSD00032 + **SGSP472**		**SGSD00033** + **SGSP362**

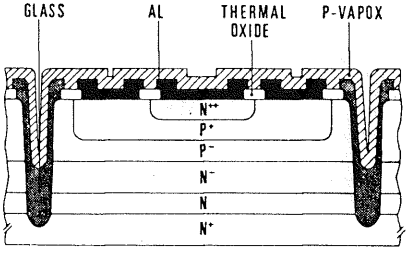
Line = 220V or 110V with voltage doubler

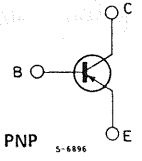
APPLICATION POWER FACTORS

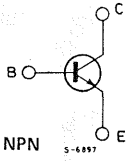
Conditions of Use	Critical Application (Computer)	Industrial Application (Office Equipment)	Consumer Use (Home)
Low Ambient or Large Heatsink	1.0	1.25	1.5
Normal Ambient or Medium Heatsink	0.8	1.0	1.25
High Ambient or Small Heatsink	0.6	0.75	1.0

INDIVIDUAL DESIGN PHILOSOPHY AND MTBF OBJECTIVES MAY MODIFY THESE FACTORS OR THE CHOICE OF DEVICE

OFF LINE SWITCHING POWER SUPPLIES POWER SWITCH TYPE: BIPOLAR TRANSISTOR MULTIEPITAXIAL MESA

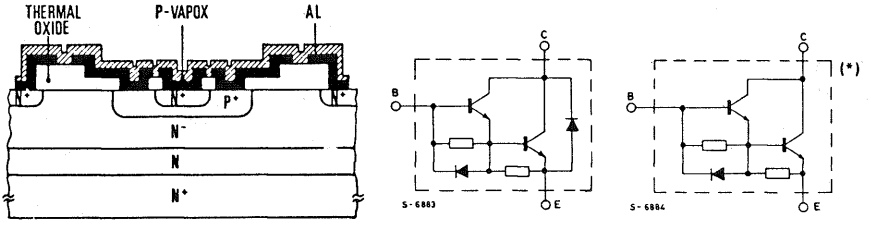






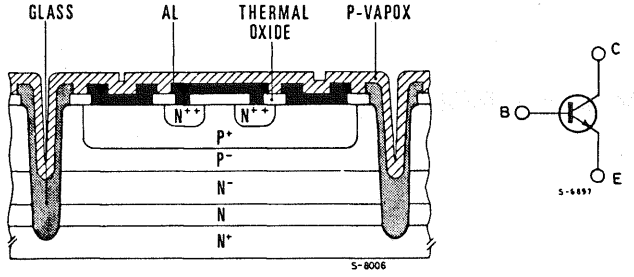
- WIDE CHOICE OF DEVICES AND PACKAGES
- 20kHz OPERATION NORMAL
- 30kHz POSSIBLE WITH CARE
- ECONOMIC AND HIGH VOLUME
- SOME PNP DEVICES AVAILABLE

OFF LINE SWITCHING POWER SUPPLIES
POWER SWITCH TYPE: BIPOLAR DARLINGTON
FAST DARLINGTON



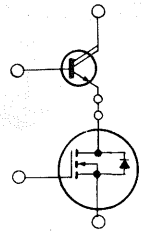
- HIGH GAIN SIMPLIFIES DRIVE CIRCUIT
- DRIVE LESS CRITICAL THAN TRANSISTOR
- 30kHz OPERATION NORMAL
- BEST CURRENT TO COST RATIO

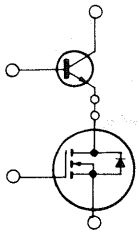
OFF LINE SWITCHING POWER SUPPLIES
POWER SWITCH TYPE: BIPOLAR TRANSISTOR
FASTSWITCH™ hollow emitter



- 50kHz OPERATION NORMAL
- > 100Hz POSSIBLE WITH CARE
- 1A TO 10A WORKING CURRENTS
- TO-220/SOT-93/TO-3 PACKAGES AVAILABLE

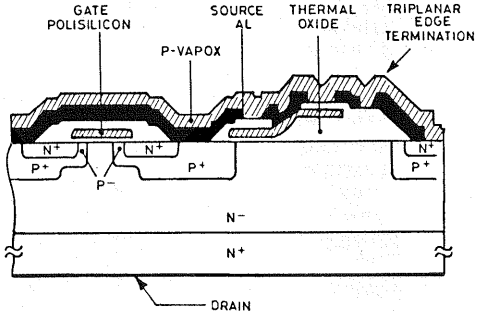
OFF LINE SWITCHING POWER SUPPLIES
POWER SWITCH TYPE: EMITTER SWITCHED BIPOLAR & POWER MOS CASCODE

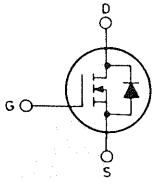

S-8182


S-8183

- SWITCHING SIMILAR TO POWER MOS > 100kHz
- POWER MOS IS ECONOMIC LOW VOLTAGE TYPE
- WITH FAST DARLINGTON DIRECT I.C. DRIVE
- EXTENDS RBSOA OF TRANSISTORS TO I_{CM}/V_{CES}
- CAN USE REGENERATIVE DRIVE TECHNIQUES

OFF LINE SWITCHING POWER SUPPLIES
POWER SWITCH TYPE: POWER MOS DMOS MULTICELL





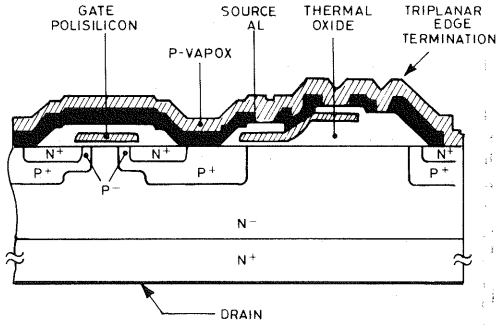
- EASY TO DRIVE AT 50kHz
- 300kHz POSSIBLE WITH CARE
- LIMITED AVAILABILITY AT > 500V
- HIGH COMPONENT COST VS BIPOLAR AT 400V
- $R_{DS\ (on)}$ INCREASES RAPIDLY WITH V_{DSS} SO 1000V PARTS ARE EXTREMELY EXPENSIVE

N-CHANNEL POWER MOS TRANSISTORS

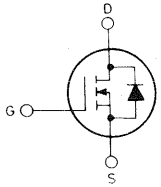
VERY FAST SWITCHING AND/OR EASY DRIVING

Very fast switching and/or easy driving:

- SMPS
- DC-DC CONVERTERS
- SYNCHRONOUS RECTIFIERS
- DRIVERS



INTERNAL SCHEMATIC DIAGRAM



SEF ≡ IRF
SEFP ≡ MTP
SEFM ≡ MTM

$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ @ (max) (Ω)	I_D (A)	Package	Type	I_D (max) (A)	P_{tot} (W)	g_{fs} (min) (℧)	C_{iss} (max) (pF)
50	0.6	2.5	TO-220	**SEFP5N05**	5.0	50	0.75	270
50	0.3	3.5	SOT-82	**SGSP258**	7.0	40	1.5	270
50	0.3	3.5	TO-220	**SGSP358**	7.0	50	1.5	270
50	0.3	3.5	TO-39	**SGSP158**	5.0	15	1.5	270
50	0.28	5.0	TO-220	**SEFP10N05**	10.0	75	2.5	550
50	0.28	5.0	TO-3	**SEFM10N05**	10.0	75	2.5	550
50	0.2	6.0	TO-220	**SEFP12N05**	12.0	75	3.0	550
50	0.2	6.0	TO-3	**SEFM12N05**	12.0	75	3.0	550
50	0.16	7.5	TO-220	**SEFP15N05**	15.0	75	3.5	550
50	0.16	7.5	TO-3	**SEFM15N05**	15.0	75	3.5	550
50	0.13	5.0	SOT-82	**SGSP222**	10.0	50	3.0	550
50	0.13	5.0	SOT-93	**SGSP422**	10.0	75	3.0	550
50	0.13	5.0	TO-220	**SGSP322**	10.0	75	3.0	550
50	0.13	5.0	TO-3	**SGSP522**	10.0	75	3.0	550
50	0.13	3.5	TO-39	**SGSP122**	7.0	15	2.5	550
50	0.12	6.0	TO-220	**BUZ10A**	12.0	75	3.0	550
50	0.12	6.0	TO-220	**BUZ71A**	12.0	40	3.0	550
50	0.1	6.0	TO-220	**BUZ10**	12.0	75	3.0	550
50	0.1	6.0	TO-220	**BUZ71**	12.0	40	3.0	550
50	0.08	12.5	TO-220	**SEFP25N05**	25.0	100	5.0	1400
50	0.08	12.5	TO-3	**SEFM25N05**	25.0	100	5.0	1400
50	0.06	12.0	SOT-93	**SGSP482**	24.0	125	5.0	1400
50	0.06	12.0	TO-220	**SGSP382**	24.0	100	5.0	1400

N-CHANNEL POWER MOS TRANSISTORS

VERY FAST SWITCHING AND/OR EASY DRIVING (continued)

$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ (max) (Ω) @	I_D (A)	Package	Type	I_D (max) (A)	P_{tot} (W)	g_{fs} (min) (℧)	C_{iss} (max) (pF)
50	0.06	12.0	TO-3	**SGSP582**	24.0	125	5.0	1400
50	0.055	17.5	SOT-93	**SEFH35N05**	35.0	150	8.0	2400
50	0.055	17.5	TO-3	**SEFM35N05**	35.0	150	8.0	2400
50	0.033	20.0	SOT-93	**SGSP492**	40.0	150	10.0	2400
50	0.033	20.0	TO-3	**SGSP592**	40.0	150	10.0	2400
60	0.8	2.0	TO-220	**SEF513**	3.5	20	1.0	270
60	0.6	2.0	TO-220	**SEF511**	4.0	20	1.0	270
60	0.6	2.5	TO-220	**SEFP5N06**	5.0	50	0.75	270
60	0.4	4.0	TO-220	**SEF523**	7.0	40	1.5	480
60	0.4	4.0	TO-3	**SEF123**	7.0	40	1.5	480
60	0.4	3.0	TO-39	**SEFF123**	5.0	20	1.5	480
60	0.3	3.5	SOT-82	**SGSP257**	7.0	40	1.5	270
60	0.3	4.0	TO-220	**SEF521**	8.0	40	1.5	480
60	0.3	3.5	TO-220	**SGSP357**	7.0	50	1.5	270
60	0.3	4.0	TO-3	**SEF121**	8.0	40	1.5	480
60	0.3	3.0	TO-39	**SEFF121**	6.0	20	1.5	480
60	0.3	3.5	TO-39	**SGSP157**	5.0	15	1.5	270
60	0.28	5.0	TO-220	**SEFP10N06**	10.0	75	2.5	550
60	0.28	5.0	TO-3	**SEFM10N06**	10.0	75	2.5	550
60	0.25	8.0	TO-220	**SEF533**	12.0	75	3.0	1200
60	0.25	8.0	TO-3	**SEF133**	12.0	75	4.0	1200
60	0.2	6.0	TO-220	**SEFP12N06**	12.0	75	3.0	550
60	0.2	6.0	TO-3	**SEFM12N06**	12.0	75	3.0	550
60	0.18	8.0	TO-220	**SEF531**	14.0	75	3.0	1200
60	0.18	8.0	TO-3	**SEF131**	14.0	75	4.0	1200
60	0.16	7.5	TO-220	**SEFP15N06**	15.0	75	3.5	1200
60	0.16	7.5	TO-3	**SEFM15N06**	15.0	75	3.5	550
60	0.13	5.0	SOT-82	**SGSP221**	10.0	50	3.0	550
60	0.13	5.0	SOT-93	**SGSP421**	10.0	75	3.0	550
60	0.13	5.0	TO-220	**SGSP321**	10.0	75	3.0	550
60	0.13	5.0	TO-3	**SGSP521**	10.0	75	3.0	550
60	0.13	3.5	TO-39	**SGSP121**	7.0	15	2.5	550
60	0.11	12.0	TO-220	**SEF543**	24.0	125	5.0	1600
60	0.11	15.0	TO-3	**SEF143**	24.0	125	6.0	2200
60	0.085	15.0	TO-220	**SEF541**	27.0	125	5.0	1600
60	0.085	15.0	TO-3	**SEF141**	27.0	125	6.0	2200
60	0.08	12.5	TO-220	**SEFP25N06**	25.0	100	5.0	1400
60	0.08	20.0	TO-3	**SEF153**	33.0	150	9.0	2200
60	0.08	12.5	TO-3	**SEFM25N06**	25.0	100	5.0	1400
60	0.06	12.0	SOT-93	**SGSP481**	24.0	125	5.0	1400
60	0.06	12.0	TO-220	**SGSP381**	24.0	100	5.0	1400
60	0.06	12.0	TO-3	**SGSP581**	24.0	125	5.0	1400
60	0.055	17.5	SOT-93	**SEFH35N06**	35.0	150	8.0	2400
60	0.055	20.0	TO-3	**SEF151**	40.0	150	9.0	2200

N-CHANNEL POWER MOS TRANSISTORS

VERY FAST SWITCHING AND/OR EASY DRIVING (continued)

$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ (max) (Ω) @	I_D (A)	Package	Type	I_D (max) (A)	P_{tot} (W)	g_{fs} (min) (℧)	C_{iss} (max) (pF)
60	0.055	17.5	TO-3	**SEFM35N06**	35.0	150	8.0	2200
60	0.05	20.0	SOT-93	**SGSP491**	40.0	150	10.0	2400
60	0.05	20.0	TO-3	**SGSP591**	40.0	150	10.0	2400
80	1.4	0.75	SOT-82	**SGSP202**	1.5	18	0.5	125
80	1.4	0.75	TO-220	**SGSP302**	1.5	18	0.5	125
80	1.4	0.75	TO-39	**SGSP102**	1.5	15	0.5	125
80	0.45	2.5	SOT-82	**SGSP252**	5.0	40	1.5	270
80	0.45	2.5	TO-220	**SGSP352**	5.0	50	1.5	270
80	0.45	2.5	TO-39	**SGSP152**	5.0	15	1.5	270
80	0.33	5.0	TO-220	**SEFP10N08**	10.0	75	2.5	480
80	0.33	5.0	TO-3	**SEFM10N08**	10.0	75	2.5	480
80	0.3	3.5	SOT-82	**SGSP212**	7.0	50	2.0	480
80	0.3	3.5	TO-220	**SGSP312**	7.0	75	2.0	480
80	0.3	3.5	TO-3	**SGSP512**	7.0	75	2.0	480
80	0.3	2.5	TO-39	**SGSP112**	5.0	15	2.0	480
80	0.25	6.0	TO-220	**SEFP12N08**	12.0	75	3.0	1200
80	0.25	6.0	TO-3	**SEFM12N08**	12.0	75	3.0	1200
80	0.1	8.0	SOT-93	**SGSP462**	16.0	125	4.5	1200
80	0.1	8.0	TO-220	**SGSP362**	16.0	100	4.5	1200
80	0.1	8.0	TO-3	**SGSP562**	16.0	125	4.5	1200
80	0.075	12.5	SOT-93	**SEFH25N08**	25.0	150	5.0	2200
80	0.075	12.5	TO-3	**SEFM25N08**	25.0	150	5.0	2200
80	0.05	15.0	SOT-93	**SGSP472**	30.0	150	9.0	2200
80	0.05	15.0	TO-3	**SGSP572**	30.0	150	9.0	2200
100	1.4	0.75	SOT-82	**SGSP201**	1.5	18	0.5	125
100	1.4	0.75	TO-220	**SGSP301**	1.5	18	0.5	125
100	1.4	0.75	TO-39	**SGSP101**	1.5	15	0.5	125
100	0.8	2.0	TO-220	**SEF512**	3.5	20	1.0	270
100	0.6	2.0	TO-220	**SEF510**	4.0	20	1.0	270
100	0.45	2.5	SOT-82	**SGSP251**	5.0	40	1.5	270
100	0.45	2.5	TO-220	**SGSP351**	5.0	50	1.5	270
100	0.45	2.5	TO-39	**SGSP151**	5.0	15	1.5	270
100	0.4	4.0	TO-220	**SEF522**	7.0	40	1.5	480
100	0.4	4.0	TO-3	**SEF122**	7.0	40	1.5	480
100	0.4	3.0	TO-39	**SEFF122**	5.0	20	1.5	480
100	0.33	5.0	TO-220	**SEFP10N10**	10.0	75	2.5	480
100	0.33	5.0	TO-3	**SEFM10N10**	10.0	75	2.0	480
100	0.3	3.5	SOT-82	**SGSP211**	7.0	50	2.0	480
100	0.3	4.0	TO-220	**SEF520**	8.0	40	1.5	480
100	0.3	3.5	TO-220	**SGSP311**	7.0	75	2.0	480
100	0.3	4.0	TO-3	**SEF120**	8.0	40	1.5	480
100	0.3	3.5	TO-3	**SGSP511**	7.0	75	2.0	480
100	0.3	3.0	TO-39	**SEFF120**	6.0	20	1.5	480

N-CHANNEL POWER MOS TRANSISTORS

VERY FAST SWITCHING AND/OR EASY DRIVING (continued)

$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ (max) (Ω) @	I_D (A)	Package	Type	I_D (max) (A)	P_{tot} (W)	g_{fs} (min) (℧)	C_{iss} (max) (pF)
100	0.3	2.5	TO-39	**SGSP111**	5.0	15	2.0	480
100	0.25	5.0	TO-220	**BUZ72A**	9.0	40	2.7	480
100	0.25	8.0	TO-220	**SEF532**	12.0	75	4.0	1200
100	0.25	6.0	TO-220	**SEFP12N10**	12.0	75	3.0	1200
100	0.25	8.0	TO-3	**SEF132**	12.0	75	4.0	1200
100	0.25	6.0	TO-3	**SEFM12N10**	12.0	75	3.0	1200
100	0.18	8.0	TO-220	**SEF530**	14.0	75	4.0	1200
100	0.18	8.0	TO-3	**SEF130**	14.0	75	4.0	1200
100	0.15	8.0	SOT-93	**SGSP461**	16.0	125	4.5	1200
100	0.15	8.0	TO-220	**SGSP361**	16.0	100	4.5	1200
100	0.15	8.0	TO-3	**SGSP561**	16.0	125	4.5	1200
100	0.11	15.0	TO-220	**SEF542**	24.0	125	5.0	1600
100	0.11	15.0	TO-3	**SEF142**	24.0	125	6.0	2200
100	0.085	15.0	TO-3	**SEF140**	27.0	125	6.0	2200
100	0.08	20.0	TO-3	**SEF152**	33.0	150	9.0	2200
100	0.075	12.5	SOT-93	**SEFH25N10**	25.0	150	5.0	2200
100	0.075	15.0	SOT-93	**SGSP471**	30.0	150	9.0	2200
100	0.075	12.5	TO-3	**SEFM25N10**	25.0	150	5.0	2200
100	0.075	15.0	TO-3	**SGSP571**	30.0	150	9.0	2200
100	0.055	20.0	TO-3	**SEF150**	40.0	150	9.0	2200
150	1.2	2.5	TO-220	**SEF623**	4.0	40	1.3	600
150	1.2	2.5	TO-3	**SEF223**	4.0	40	1.3	600
150	0.8	2.5	TO-220	**SEF621**	5.0	40	1.3	600
150	0.8	2.5	TO-3	**SEF221**	5.0	40	1.3	600
150	0.6	5.0	TO-220	**SEF633**	8.0	75	3.0	1200
150	0.6	5.0	TO-3	**SEF233**	8.0	75	3.0	1200
150	0.4	5.0	TO-220	**SEF631**	9.0	75	3.0	1200
150	0.4	5.0	TO-3	**SEF231**	9.0	75	3.0	1200
150	0.22	10.0	TO-3	**SEF243**	16.0	125	6.0	2200
150	0.18	10.0	TO-3	**SEF241**	18.0	125	6.0	2200
180	1.0	2.5	TO-220	**SEFP5N18**	5.0	75	1.5	500
180	1.0	2.5	TO-3	**SEFM5N18**	5.0	75	1.5	500
180	0.4	4.0	TO-220	**SEFP8N18**	8.0	75	3.0	1200
180	0.4	4.0	TO-3	**SEFM8N18**	8.0	75	3.0	1200
180	0.16	7.5	SOT-93	**SEFH15N18**	15.0	150	4.0	2500
180	0.16	7.5	TO-3	**SEFM15N18**	15.0	150	4.0	2500
200	1.2	2.5	TO-220	**SEF622**	4.0	40	1.3	600
200	1.2	2.5	TO-3	**SEF222**	4.0	40	1.3	600
200	1.0	2.5	TO-220	**SEFP5N20**	5.0	75	1.5	500
200	1.0	2.5	TO-3	**SEFM5N20**	5.0	75	1.5	500
200	0.8	2.5	TO-220	**SEF620**	5.0	40	1.3	600
200	0.8	2.5	TO-3	**SEF220**	5.0	40	1.3	600
200	0.75	3.0	SOT-82	**SGSP217**	6.0	50	1.5	500

N-CHANNEL POWER MOS TRANSISTORS

VERY FAST SWITCHING AND/OR EASY DRIVING (continued)

$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ (max) (Ω)	@ I_D (A)	Package	Type	I_D (max) (A)	P_{tot} (W)	g_{fs} (min) (℧)	C_{iss} (max) (pF)
200	0.75	3.0	TO-220	**SGSP317**	6.0	75	1.5	500
200	0.75	3.0	TO-3	**SGSP517**	6.0	75	1.5	500
200	0.75	2.0	TO-39	**SGSP117**	4.0	15	1.5	500
200	0.6	5.0	TO-220	**SEF632**	8.0	75	3.0	1200
200	0.6	5.0	TO-3	**SEF232**	8.0	75	3.0	1200
200	0.4	5.0	TO-220	**SEF630**	9.0	75	3.0	1200
200	0.4	4.0	TO-220	**SEFP8N20**	8.0	75	3.0	1200
200	0.4	5.0	TO-3	**SEF230**	9.0	75	3.0	1200
200	0.4	4.0	TO-3	**SEFM8N20**	8.0	75	3.0	1200
200	0.33	5.0	SOT-93	**SGSP467**	10.0	100	6.5	1200
200	0.33	5.0	TO-220	**SGSP367**	10.0	100	6.5	1200
200	0.33	5.0	TO-3	**SGSP567**	10.0	125	6.5	1200
200	0.22	10.0	TO-3	**SEF242**	16.0	125	6.0	2200
200	0.18	10.0	TO-3	**SEF240**	18.0	125	6.0	2200
200	0.17	10.0	SOT-93	**SGSP477**	20.0	150	8.0	2200
200	0.17	10.0	TO-3	**SGSP577**	20.0	150	8.0	2200
200	0.16	7.5	SOT-93	**SEFH15N20**	15.0	150	4.0	2500
200	0.16	7.5	TO-3	**SEFM15N20**	15.0	150	4.0	2500
250	1.2	3.0	SOT-82	**SGSP216**	6.0	50	1.5	500
250	1.2	3.0	TO-220	**SGSP316**	6.0	75	1.5	500
250	1.2	3.0	TO-3	**SGSP516**	6.0	75	1.5	500
250	1.2	2.0	TO-39	**SGSP116**	4.0	15	1.5	500
250	0.45	5.0	SOT-93	**SGSP463**	10.0	100	6.5	1200
250	0.45	5.0	TO-220	**SGSP363**	10.0	100	6.5	1200
250	0.45	5.0	TO-3	**SGSP563**	10.0	125	6.5	1200
250	0.22	10.0	SOT-93	**SGSP473**	20.0	150	8.0	2200
250	0.22	10.0	TO-3	**SGSP573**	20.0	150	8.0	2200
350	20.0	0.3	SOT-82	**SGSP242**	0.6	18	0.2	105
350	20.0	0.3	TO-220	**SGSP342**	0.6	18	0.2	105
350	20.0	0.3	TO-39	**SGSP142**	0.6	15	0.2	105
350	5.0	0.75	SOT-82	**SGSP256**	1.5	40	0.85	250
350	5.0	0.8	TO-220	**SEF713**	1.3	20	0.5	450
350	5.0	0.75	TO-220	**SGSP356**	1.5	50	0.85	250
350	5.0	0.75	TO-39	**SGSP156**	1.5	15	0.85	250
350	3.6	0.8	TO-220	**SEF711**	1.5	20	0.5	450
350	3.3	1.5	TO-220	**SEFP3N35**	3.0	75	0.75	450
350	3.3	1.5	TO-3	**SEFM3N35**	3.0	75	0.75	450
350	2.5	1.5	SOT-82	**SGSP232**	3.0	50	1.5	450
350	2.5	1.5	TO-220	**SEF723**	2.5	40	1.0	1000
350	2.5	1.5	TO-220	**SGSP332**	3.0	75	1.5	450
350	2.5	1.5	TO-3	**SEF323**	2.5	40	1.0	1000
350	2.5	1.5	TO-3	**SGSP532**	3.0	75	1.5	450
350	2.5	1.5	TO-39	**SGSP132**	3.0	15	1.5	450

N-CHANNEL POWER MOS TRANSISTORS

VERY FAST SWITCHING AND/OR EASY DRIVING (continued)

$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ (max) (Ω) @	I_D (A)	Package	Type	I_D (max) (A)	P_{tot} (W)	g_{fs} (min) (℧)	C_{iss} (max) (pF)
350	2.0	2.5	TO-220	**SEFP5N35**	5.0	75	2.0	1000
350	1.8	1.5	TO-220	**SEF721**	3.0	40	1.0	1000
350	1.8	1.5	TO-3	**SEF321**	3.0	40	1.0	1000
350	1.5	3.0	TO-220	**SEF733**	4.5	75	3.0	1000
350	1.5	3.0	TO-3	**SEF333**	4.5	75	3.0	1000
350	1.0	3.0	SOT-93	**SGSP466**	6.0	125	3.0	1000
350	1.0	3.0	TO-220	**SEF731**	5.5	75	3.0	1000
350	1.0	3.0	TO-220	**SGSP366**	6.0	100	3.0	1000
350	1.0	3.0	TO-3	**SEF331**	5.5	75	3.0	1000
350	1.0	2.5	TO-3	**SEFM5N35**	5.0	75	2.0	1000
350	1.0	3.0	TO-3	**SGSP566**	6.0	125	3.0	1000
350	0.8	4.0	SOT-93	**SEFH8N35**	8.0	150	3.0	2100
350	0.8	5.0	TO-3	**SEF343**	8.0	125	4.0	2100
350	0.8	4.0	TO-3	**SEFM8N35**	8.0	150	3.0	2100
350	0.55	6.0	SOT-93	**SGSP476**	12.0	150	6.0	2100
350	0.55	5.0	TO-3	**SEF341**	10.0	125	4.0	2100
350	0.55	6.0	TO-3	**SGSP576**	12.0	150	6.0	2100
400	20.0	0.3	SOT-82	**SGSP241**	0.6	18	0.2	105
400	20.0	0.3	TO-220	**SGSP341**	0.6	75	0.2	105
400	20.0	0.3	TO-39	**SGSP141**	0.6	15	0.2	105
400	5.0	0.75	SOT-82	**SGSP255**	1.5	40	0.85	250
400	5.0	0.75	TO-220	**SGSP355**	1.5	50	0.85	250
400	5.0	0.75	TO-39	**SGSP155**	1.5	15	0.85	250
400	3.6	0.8	TO-220	**SEF710**	1.5	20	0.5	450
400	3.6	0.8	TO-220	**SEF712**	1.3	20	0.5	450
400	3.3	1.5	TO-220	**SEFP3N40**	3.0	75	0.75	450
400	3.3	1.5	TO-3	**SEFM3N40**	3.0	75	0.75	450
400	2.5	1.5	SOT-82	**SGSP231**	3.0	50	1.5	450
400	2.5	1.5	TO-220	**BUZ76A**	2.6	40	2.0	450
400	2.5	1.5	TO-220	**SEF722**	2.5	40	1.0	1000
400	2.5	1.5	TO-220	**SGSP331**	3.0	75	1.5	450
400	2.5	1.5	TO-3	**SEF322**	2.5	40	1.0	1000
400	2.5	1.5	TO-3	**SGSP531**	3.0	75	1.5	450
400	2.5	1.5	TO-39	**SGSP131**	3.0	15	1.5	450
400	1.8	1.5	TO-220	**BUZ76**	3.0	40	2.0	450
400	1.8	1.5	TO-220	**SEF720**	3.0	40	1.0	1000
400	1.8	1.5	TO-3	**SEF320**	3.0	40	1.0	1000
400	1.5	3.0	TO-220	**SEF732**	4.5	75	3.0	1000
400	1.5	3.0	TO-3	**SEF332**	4.5	75	3.0	1000
400	1.0	3.0	SOT-93	**SGSP465**	6.0	125	3.0	1000
400	1.0	3.0	TO-220	**SEF730**	5.5	75	3.0	1000
400	1.0	2.5	TO-220	**SEFP5N40**	5.0	75	2.0	1000
400	1.0	3.0	TO-220	**SGSP365**	6.0	100	3.0	1000
400	1.0	3.0	TO-3	**SEF330**	5.5	75	3.0	1000

N-CHANNEL POWER MOS TRANSISTORS

VERY FAST SWITCHING AND/OR EASY DRIVING (continued)

$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ (max) (Ω)	@ I_D (A)	Package	Type	I_D (max) (A)	P_{tot} (W)	g_{fs} (min) (℧)	C_{iss} (max) (pF)
400	1.0	2.5	TO-3	**SEFM5N40**	5.0	75	2.0	1000
400	1.0	3.0	TO-3	**SGSP565**	6.0	125	3.0	1000
400	0.8	5.0	TO-3	**SEF342**	8.0	125	4.0	2100
400	0.55	4.0	SOT-93	**SEFH8N40**	8.0	150	3.0	2100
400	0.55	6.0	SOT-93	**SGSP475**	12.0	150	6.0	2100
400	0.55	5.0	TO-3	**SEF340**	10.0	125	4.0	2100
400	0.55	4.0	TO-3	**SEFM8N40**	8.0	150	3.0	2100
400	0.55	6.0	TO-3	**SGSP575**	12.0	150	6.0	2100
450	20.0	0.3	SOT-82	**SGSP240**	0.6	18	0.2	105
450	20.0	0.3	TO-220	**SGSP340**	0.6	18	0.2	105
450	20.0	0.3	TO-39	**SGSP140**	0.6	15	0.2	105
450	6.5	0.75	SOT-82	**SGSP254**	1.5	40	0.85	250
450	6.5	0.75	TO-220	**SGSP354**	1.5	50	0.85	250
450	6.5	0.75	TO-39	**SGSP154**	1.5	15	0.85	250
450	4.0	1.0	TO-220	**SEF823**	2.0	40	1.0	800
450	4.0	1.0	TO-220	**SEFP2N45**	2.0	75	1.0	500
450	4.0	1.0	TO-3	**SEF423**	2.0	40	1.0	800
450	4.0	1.0	TO-3	**SEFM2N45**	4.0	75	1.0	500
450	3.0	1.5	SOT-82	**SGSP230**	3.0	50	1.5	450
450	3.0	1.0	TO-220	**SEF821**	2.5	40	1.0	800
450	3.0	1.5	TO-220	**SGSP330**	3.0	75	1.5	450
450	3.0	1.0	TO-3	**SEF421**	2.5	40	1.0	800
450	3.0	1.5	TO-3	**SGSP530**	3.0	75	1.5	450
450	3.0	1.5	TO-39	**SGSP130**	3.0	15	1.5	450
450	2.0	2.5	TO-220	**SEF833**	4.0	75	2.5	1200
450	2.0	2.5	TO-3	**SEF433**	4.0	75	2.5	1200
450	1.5	3.0	SOT-93	**SGSP464**	6.0	125	3.0	1000
450	1.5	2.5	TO-220	**SEF830**	4.5	75	2.5	1200
450	1.5	2.5	TO-220	**SEF831**	4.5	75	2.5	1200
450	1.5	2.0	TO-220	**SEFP4N45**	4.0	75	1.5	1000
450	1.5	3.0	TO-220	**SGSP364**	6.0	100	3.0	1000
450	1.5	2.5	TO-3	**SEF431**	4.5	75	2.5	1200
450	1.5	2.0	TO-3	**SEFM4N45**	4.0	75	1.5	1000
450	1.5	3.0	TO-3	**SGSP564**	6.0	125	3.0	1000
450	1.1	4.0	TO-3	**SEF443**	7.0	125	4.0	2100
450	0.85	4.0	TO-3	**SEF441**	8.0	125	4.0	2100
450	0.8	3.5	SOT-93	**SEFH7N45**	7.0	150	2.0	2100
450	0.7	6.0	SOT-93	**SGSP474**	12.0	150	6.0	2100
450	0.8	3.5	TO-3	**SEFM7N45**	7.0	150	2.0	2100
450	0.7	6.0	TO-3	**SGSP574**	12.0	150	6.0	2100
500	40.0	0.3	SOT-82	**SGSP249**	0.5	18	0.2	105
500	40.0	0.3	TO-220	**SGSP349**	0.5	18	0.2	105
500	40.0	0.3	TO-39	**SGSP149**	0.5	15	0.2	105

N-CHANNEL POWER MOS TRANSISTORS

VERY FAST SWITCHING AND/OR EASY DRIVING (continued)

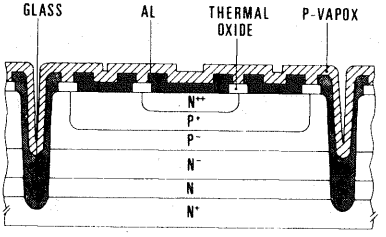
$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ (max) (Ω) @	I_D (A)	Package	Type	I_D(max) (A)	P_{tot} (W)	g_{fs}(min) (℧)	C_{iss}(max) (pF)
500	8.5	0.6	SOT-82	**SGSP239**	1.2	40	0.85	250
500	8.5	0.6	TO-220	**SGSP339**	1.2	50	0.85	250
500	8.5	0.6	TO-39	**SGSP139**	1.2	15	0.85	250
500	4.0	1.0	TO-220	**SEF822**	2.0	40	1.0	800
500	4.0	1.0	TO-3	**SEF422**	2.0	40	1.0	800
500	3.8	1.0	SOT-82	**SGSP219**	2.0	50	1.2	380
500	3.8	1.0	TO-220	**SGSP319**	2.0	75	1.2	380
500	3.8	1.0	TO-3	**SGSP519**	2.0	75	1.2	380
500	3.8	1.0	TO-39	**SGSP119**	2.0	15	1.2	380
500	3.0	1.0	TO-220	**SEF820**	2.5	40	1.0	800
500	3.0	1.0	TO-3	**SEF420**	2.5	40	1.0	800
500	2.0	2.5	TO-220	**SEF832**	4.0	75	2.5	1200
500	2.0	2.5	TO-3	**SEF432**	4.0	75	2.5	1200
500	1.75	2.5	SOT-93	**SGSP469**	5.0	125	3.0	800
500	1.75	2.5	TO-220	**SGSP369**	5.0	100	3.0	800
500	1.75	2.5	TO-3	**SGSP569**	5.0	125	3.0	800
500	1.5	2.0	TO-220	**SEFP4N50**	4.0	75	1.5	1200
500	1.5	2.5	TO-3	**SEF430**	4.5	75	2.5	1200
500	1.5	2.0	TO-3	**SEFM4N50**	4.0	75	1.5	1200
500	1.1	4.0	TO-3	**SEF442**	7.0	125	4.0	2100
500	0.85	4.0	TO-3	**SEF440**	8.0	125	4.0	2100
500	0.8	3.5	SOT-93	**SEFH7N50**	7.0	150	2.0	1900
500	0.8	3.5	TO-3	**SEFM7N50**	7.0	150	2.0	1900
500	0.7	5.0	SOT-93	**SGSP479**	10.0	150	5.0	1900
500	0.7	5.0	TO-3	**SGSP579**	10.0	150	5.0	1900
550	40.0	0.3	SOT-82	**SGSP248**	0.5	18	0.2	105
550	40.0	0.3	TO-220	**SGSP348**	0.5	18	0.2	105
550	40.0	0.3	TO-39	**SGSP148**	0.5	15	0.2	105
550	11.0	0.6	SOT-82	**SGSP238**	1.2	40	0.85	250
550	11.0	0.6	TO-220	**SGSP338**	1.2	50	0.85	250
550	11.0	0.6	TO-39	**SGSP138**	1.2	15	0.85	250
550	4.5	1.0	SOT-82	**SGSP218**	2.0	50	1.2	380
550	4.5	1.0	TO-220	**SGSP318**	2.0	75	1.2	380
550	4.5	1.0	TO-3	**SGSP518**	2.0	75	1.2	380
550	4.5	1.0	TO-39	**SGSP118**	2.0	15	1.2	380
550	2.5	2.5	SOT-93	**SGSP468**	5.0	125	3.0	800
550	2.5	1.5	TO-220	**SEFP3N55**	3.0	75	1.5	1200
550	2.5	2.5	TO-220	**SGSP368**	5.0	100	3.0	800
550	2.5	1.5	TO-3	**SEFM3N55**	2.5	75	1.5	1600
550	2.5	2.5	TO-3	**SGSP568**	5.0	125	3.0	800
550	1.5	3.0	SOT-93	**SEFH6N55**	6.0	150	2.0	1900
550	1.5	3.0	TO-3	**SEFM6N55**	6.0	150	2.0	1900
550	1.0	5.0	SOT-93	**SGSP478**	10.0	150	5.0	1900
550	1.0	5.0	TO-3	**SGSP578**	10.0	150	5.0	1900

POWER TRANSISTORS

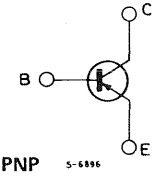
HIGH VOLTAGE FAST SWITCHING

MULTIEPITAXIAL MESA - I_{CM} 1.5 to 30A; V_{CEO} 300 to 700V

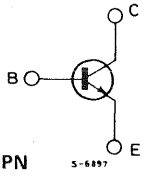
NPN and PNP types
High voltage (V_{CBO} up to 1200V)
High power
Very good $I_{s/b}$ and $E_{s/b}$ performance
High switching speed
Good stability



INTERNAL SCHEMATIC DIAGRAMS



PNP 5-6896



NPN 5-6897

MULTIEPITAXIAL MESA

I_C (A)	V_{CBO} (V)	V_{CEO} (V)	P_{tot} (W)	Package	TYPE NPN	TYPE PNP	@ h_{FE} (min)	@ I_C (A)	@ V_{CE} (V)	V_{CEsat} max (V)	@ I_C (A)	@ I_B (mA)
1.5	600	300	50	SOT-82	**SGS13002**		5	1	2	1	1	250
1.5	600	300	50	TO-220	**SGS13002T**		5	1	2	1	1	250
1.5	700	400	50	SOT-82	**SGS13003**		5	1	2	1	1	250
1.5	700	400	50	TO-220	**SGS13003T**		5	1	2	1	1	250
2	800	400	40	TO-220	**BUX84**		5	1	3	1.5	0.3	30
2	800	400	40	TO-220	**BUX84A**		5	1	1	0.8	0.3	30
2	1000	450	40	TO-220	**BUX85**		5	1	1	1	1	200
4	600	300	75	TO-220	**MJE13004**		10	1	5	0.6	2	500
4	700	400	75	TO-220	**MJE13005**		10	1	5	0.6	2	500
5	350	250	80	TO-220	**2N6497**		10	2.5	10	1	1.5	500
5	350	250	100	SOT-93	**TIP51**		10	3	10	1.5	3	600
5	400	300	80	TO-220	**2N6498**		10	2	10	1.25	2.5	500
5	400	300	100	SOT-93	**TIP52**		10	3	10	1.5	3	600
5	450	350	80	TO-220	**2N6499**		10	2.5	10	1.5	2.5	500
5	450	350	100	SOT-93	**TIP53**		10	3	10	1.5	3	600
5	500	400	100	SOT-93	**TIP54**		10	3	10	1.5	3	600
5	850	400	85	TO-220	**BUV46**		5	3.5	5	1.5	2.5	500

POWER TRANSISTORS

MULTIEPITAXIAL MESA (continued)

I_C (A)	V_{CBO} (V)	V_{CEO} (V)	P_{tot} (W)	Package	TYPE NPN	TYPE PNP	@ h_{FE} (min)	@ I_C (A)	@ V_{CE} (V)	V_{CEsat} max (V)	@ I_C (A)	@ I_B (mA)
5	850	400	100	TO-220	**BUT11**		5	3	1.5	1.5	3	600
5	850	400	100	SOT-93	**BUW11**		5	3	1.5	1.5	3	600
5	1000	450	100	TO-220	**BUT11A**		5	2.5	1.5	1.5	2.5	500
5	1000	450	100	SOT-93	**BUW11A**		5	2.5	1.5	1.5	2.5	500
6	400	350	60	TO-220		**BUW22P**	12	0.5	5	1.5	2.5	1000
6	400	350	75	TO-3		**BUW22**	12	0.5	5	1.5	2.5	1000
6	450	400	60	TO-220		**BUW22AP**	12	0.5	5	1.5	2.5	1000
6	450	400	75	TO-3		**BUW22A**	12	0.5	5	1.5	2.5	1000
6	800	375	75	TO-3	**BU326***		25	1	5	1.5	2.5	500
6	800	375	113	SOT-93	**BU426***		25	1	5	1.5	2.5	500
6	800	400	60	TO-3	**BU326S**		3.5	4	5	1.5	2.5	500
6	900	400	75	TO-3	**BU326A***		15	1	5	1.5	2.5	500
6	900	400	113	SOT-93	**BU426A***		15	0.6	5	1.5	2.5	500
8	600	300	80	TO-220	**MJE13006**		8	2	5	1.5	5	1000
8	450	400	80	TO-220		**MJE5852**	15	2	5	2	4	1000
8	450	400	120	TO-3	**BUX44**		8	4	4	1.5	4	800
8	700	400	80	TO-220	**MJE13007**		8	2	5	1.5	5	1000
8	850	400	80	TO-220	**MJE13007A**		8	2	5	1.5	5	1000
8	850	400	125	SOT-93	**BUW12**		5	6	1.5	1.5	6	1200
8	850	400	125	TO-3	**BUS12**		5	6	1.5	1,5	6	1200
8	850	400	125	TO-3	**2N6545**		4	8	5	1.5	5	1000
8	1000	450	125	SOT-93	**BUW12A**		5	5	1.5	1.5	5	1000
8	1000	450	125	TO-3	**BUS12A**		5	5	1.5	1.5	5	1000
9	850	400	120	SOT-93	**BUV47**		3.2	8	3	1.5	5	1000
9	850	400	125	TO-3	**BUX47**		3	9	3	1.5	6	1200
9	1000	450	120	SOT-93	**BUV47A**		3.2	8	3	1.5	5	1000
9	1000	450	120	TO-3	**BUX47A**		3	9	3	1.5	6	1200
10	800	325	100	TO-3	**BUY69B**		15	2.5	10	3.3	8	2500
10	400	350	105	TO-220		**BUW32P**	12	1	5	1.5	5	1500
10	400	350	125	TO-3		**BUW32**	12	1	5	1.5	5	1500
10	450	400	105	TO-220		**BUW32AP**	12	1	5	1.5	5	1500
10	450	400	125	TO-3		**BUW32A**	12	1	5	1.5	5	1500
10	325	400	120	TO-3	**BUX43**		8	5	4	2	5	1000
10	450	400	150	TO-3	**BUX14**		8	6	4	1.6	6	1200
10	500	400	125	TO-3	**BUW34**		15	1	5	1.5	5	1000
10	800	400	100	TO-3	**BUX80**		5	5	1.5	1.5	5	1000
10	800	400	125	TO-3	**BUW35**		15	1	5	1.5	5	1000
10	1000	400	100	TO-3	**BUY69A**		15	2.5	10	3.3	8	2500
10	900	450	125	TO-3	**BUW36**		15	1	5	1.5	5	1000
12	600	300	100	TO-220	**MJE13008**		8	5	5	1.5	8	1600
12	700	400	100	TO-220	**MJE13009**		8	5	5	1.5	8	1600

POWER TRANSISTORS

MULTIEPITAXIAL MESA (continued)

I_C (A)	V_{CBO} (V)	V_{CEO} (V)	P_{tot} (W)	Package	TYPE NPN	TYPE PNP	@ h_{FE} (min)	@ I_C (A)	V_{CE} (V)	@ V_{CEsat} max (V)	@ I_C (A)	I_B (mA)
15	400	350	105	TO-220		**BUW42P**	12	3	5	1.5	10	3000
15	400	350	150	TO-3		**BUW42**	12	3	5	1.5	10	3000
15	450	400	105	TO-220		**BUW42AP**	12	3	5	1.5	10	3000
15	450	400	150	TO-3		**BUW42A**	12	3	5	1.5	10	3000
15	400	325	160	TO-3	**BUX13**		8	8	4	1.5	8	1600
15	500	400	175	TO-3	**BUW44**		6	6	1.5	3	10	2000
15	800	400	175	TO-3	**BUW45**		7	7	1.5	1.5	10	2000
15	850	400	150	SOT-93	**BUW13**		5	10	1.5	1.5	10	2000
15	850	400	150	SOT-93	**BUV48**		5	15	5	1.5	10	2000
15	850	400	175	TO-3	**2N6547**		5	15	5	1.5	10	2000
15	850	400	175	TO-3	**BUX48**		5	15	3	1.5	10	2000
15	850	400	175	TO-3	**BUS13**		5	10	2	1.5	10	2000
15	900	450	175	TO-3	**BUW46**		7	7	1.5	1.5	10	2000
15	1000	450	150	SOT-93	**BUV48A**		5	12	5	1.5	8	1600
15	1000	450	150	SOT-93	**BUW13A**		5	8	1.5	1.5	8	1600
15	1000	450	175	TO-3	**BUX48A**		5	12	3	1.5	8	1600
15	1000	450	175	TO-3	**BUS13A**		5	8	1.6	1.8	8	1600
15	500	500	250	TO-3	**BUV25**		15	4	4	1	8	1600
15	1200	600	150	SOT-93	**BUV48B**		15	1	10	2	8	2500
15	1200	600	175	TO-3	**BUX48B**		15	1	10	2	8	2500
15	1200	700	150	SOT-93	**BUV48C**		2.5	10	3	1.5	6	1500
15	1200	700	175	TO-3	**BUX48C**		2.5	10	3	1.5	6	1500
20	450	400	250	TO-3	**BUV24**		15	6	4	1	12	2400
30	400	325	250	TO-3	**BUV23**		15	8	4	1	16	3200
30	850	400	250	TO-3	**BUS14**		5	20	1.5	1.5	20	4000
30	850	400	250	TO-3	**BUX98**		5	20	1.5	1.5	20	4000
30	1000	450	250	TO-3	**BUS14A**		5	16	1.5	1.5	16	3200
30	1000	450	250	TO-3	**BUX98A**		5	16	1.5	1.5	16	3200
30	500	500	350	TO-3	**BUX25**		8	8	4	1	8	1600
30	1000	600	250	TO-3	**BUX98B**		4	12	1.5	1.5	12	3000
30	1200	700	250	TO-3	**BUX98C**		4	12	1.5	1.5	12	3000

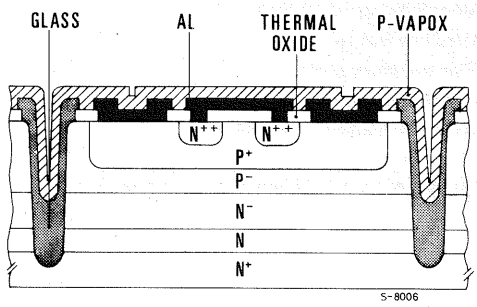
* h_{FE} is typical

POWER TRANSISTORS

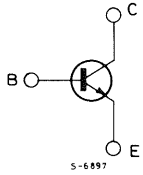
HIGH VOLTAGE VERY FAST SWITCHING

MULTIEPITAXIAL MESA FASTSWITCH™ - I_{CM} 5 to 12A; V_{CEO} 400 to 450V

Suitable for 50KHz to 100KHz switching power supplies
NPN types
High voltage (V_{CBO} up to 1000V)
High power
Very good $I_{s/b}$ and $E_{s/b}$ performance
Very high switching speed
Good stability



INTERNAL SCHEMATIC DIAGRAM



MULTIEPITAXIAL MESA FASTSWITCH™ (NPN)

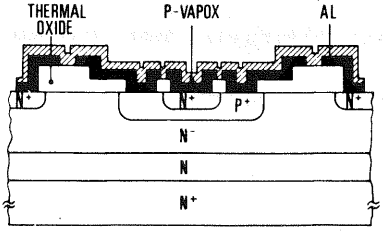
I_C (A)	V_{CBO} (V)	V_{CEO} (V)	P_{tot} (W)	Package	TYPE	@ h_{FE} (min)	@ I_C (A)	@ V_{CE} (V)	V_{CEsat} max (V)	@ I_C (A)	@ I_B (mA)
5	700	400	90	TO-220	**SGSD00042**	4	4	1	1	4	1000
5	1000	450	90	TO-220	**SGSD00044**	4	3.2	1	1	3.2	800
8	700	400	90	TO-220	**SGSD00040**	5	6	1.5	1.5	6	1200
8	700	400	120	SOT-93	**SGSD00037**	5	6	1.5	1.5	6	1200
8	700	400	120	TO-3	**SGSD00036**	5	6	1.5	1.5	6	1200
8	1000	450	90	TO-220	**SGSD00041**	5	6	1.5	1.5	6	1200
8	1000	450	120	SOT-93	**SGSD00039**	5	6	1.5	1.5	6	1200
8	1000	450	120	TO-3	**SGSD00038**	5	6	1.5	1.5	6	1200
12	700	400	150	SOT-93	**SGSD00033**	5	10	1.5	1.5	10	2000
12	700	400	175	TO-3	**SGSD00032**	5	10	1.5	1.5	10	2000
12	1000	450	150	SOT-93	**SGSD00035**	5	8	1.5	1.5	8	1600
12	1000	450	175	TO-3	**SGSD00034**	5	8	1.5	1.5	8	1600

POWER DARLINGTONS

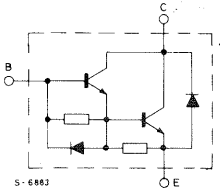
HIGH VOLTAGE FAST SWITCHING

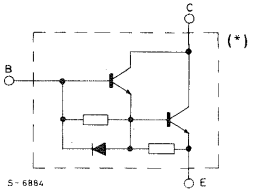
MULTIEPITAXIAL PLANAR - I_{CM} 2 to 28A; V_{CEO} 350 to 400V

NPN types
I_C range up to 28A
Monolithic speed-up diode
Very low leakage
High switching speed
High $E_{s/b}$ capability
Total base-collector passivation



INTERNAL SCHEMATIC DIAGRAMS





MULTIEPITAXIAL PLANAR (NPN)

I_C (A)	V_{CBO} (V)	V_{CEO} (V)	P_{tot} (W)	Package	TYPE	@ h_{FE} (min)	@ I_C (A)	@ V_{CE} (V)	V_{CEsat} max (V)	@ I_C (A)	@ I_B (mA)
3	600	400	35	SOT-32	**BU801**	100	1	3	2.2	1	15
7	600	400	75	TO-220	**BU810**	100	2	2	2.5	4	200
16	450	350	125	SOT-93	**SGS10004P**	40	8	5	1.8	8	400
16	450	350	175	TO-3	**SGS10004**	40	8	5	1.8	8	400
16	500	400	125	SOT-93	**SGS10005P**	40	8	5	1.8	8	400
16	500	400	175	TO-3	**SGS10005**	40	8	5	1.8	8	400
20	400	350	150	SOT-93	**MJ10004P**	50	5	5	1.9	10	400
20	400	350	175	TO-3	**MJ10004**	50	5	5	1.9	10	400
20	450	400	150	SOT-93	**MJ10005P**	50	5	5	1.9	10	400
20	450	400	175	TO-3	**MJ10005**	50	5	5	1.9	10	400
28	650	400	150	SOT-93	**SGSD00030** *	120	12	2.5	2.5	12	100
28	650	400	150	TO-3	**SGSD00031** *	120	12	2.5	2.5	12	100
28	600	400	150	SOT-93	**SGSD311** *	30	10	5	2.5	18	1800
28	600	400	150	TO-3	**SGSD310** *	30	10	5	2.5	18	1800

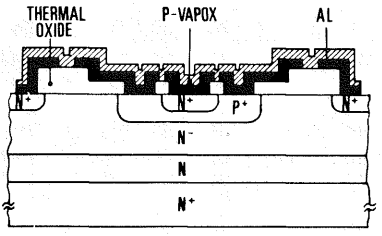
*Without parasitic CE diode

POWER TRANSISTORS

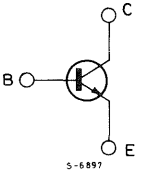
HIGH POWER FAST SWITCHING

MULTIEPITAXIAL PLANAR - I_{CM} 1 to 70A; V_{CEO} 30 to 400V

NPN types
I_C range up to 70A
Good h_{FE} linearity
Very low leakage
High switching speed
High $E_{s/b}$ capability
Total base-collector passivation



INTERNAL SCHEMATIC DIAGRAM



MULTIPEPITAXIAL PLANAR (NPN)

I_C (A)	V_{CBO} (V)	V_{CEO} (V)	P_{tot} (W)	Package	TYPE	@ h_{FE} (min)	@ I_C (A)	@ V_{CE} (V)	V_{CEsat} max (V)	@ I_C (A)	I_B (mA)
1	350	250	40	TO-220	**TIP47**	10	1	10	1	1	200
1	400	300	40	TO-220	**TIP48**	10	1	10	1	1	200
1	450	350	40	TO-220	**TIP49**	10	1	10	1	1	200
1	500	400	40	TO-220	**TIP50**	10	1	10	1	1	200
3	200	200	25	SOT-32	**BU325**	30	0.5	5	1.5	0.5	50
3	250	200	15	SOT-32	**BUY49P**	40	0.5	5	0.2	0.5	50
4	40	30	30	TO-220	**D44C1**	25	0.2	1	0.5	1	100
4	40	30	30	TO-220	**D44C2**	100	0.2	1	0.5	1	50
4	40	30	30	TO-220	**D44C3**	40	0.2	1	0.5	1	50
4	55	45	30	TO-220	**D44C4**	25	0.2	1	0.5	1	100
4	55	45	30	TO-220	**D44C5**	100	0.2	1	0.5	1	50
4	55	45	30	TO-220	**D44C6**	40	0.2	1	0.5	1	50
4	70	60	30	TO-220	**D44C7**	25	0.2	1	0.5	1	100
4	70	60	30	TO-220	**D44C8**	100	0.2	1	0.5	1	50
4	70	60	30	TO-220	**D44C9**	40	0.2	1	0.5	1	50
4	90	80	30	TO-220	**D44C10**	25	0.2	1	0.5	1	100
4	90	80	30	TO-220	**D44C11**	100	0.2	1	0.5	1	50
4	90	80	30	TO-220	**D44C12**	40	0.2	1	0.5	1	50
4	200	125	31	TO-220	**D44Q1**	30	0.2	10	1	2	200
4	250	175	31	TO-220	**D44Q3**	30	0.2	10	1	2	200
4	300	225	31	TO-220	**D44Q5**	30	0.2	10	1	2	200

POWER TRANSISTORS

MULTIEPITAXIAL PLANAR (continued)

I_C (A)	V_{CBO} (V)	V_{CEO} (V)	P_{tot} (W)	Package	TYPE	@ h_{FE} (min)	@ I_C (A)	@ V_{CE} (V)	V_{CEsat} max (V)	@ I_C (A)	I_B (mA)
7	140	90	50	TO-220	**2N6702**	20	5	2	0.8	5	500
10	30	30	50	TO-220	**D44H1**	35	2	1	1	8	800
10	30	30	50	TO-220	**D44H2**	60	2	1	1	8	400
10	45	45	50	TO-220	**D44H4**	35	2	1	1	8	800
10	45	45	50	TO-220	**D44H5**	60	2	1	1	8	400
10	60	60	50	TO-220	**D44H7**	35	2	1	1	8	800
10	60	60	50	TO-220	**D44H8**	60	2	1	1	8	400
10	80	80	50	TO-220	**D44H10**	35	2	1	1	8	800
10	80	80	50	TO-220	**D44H11**	60	2	1	1	8	400
12	300	250	120	TO-3	**BUX42**	8	6	4	1.2	4	400
15	250	200	120	TO-3	**BUX41**	8	8	4	1.2	4	400
18	220	160	120	TO-3	**BUX41N**	8	12	4	1.2	8	800
20	120	75	140	TO-3	**2N5039**	20	10	5	1	10	1000
20	160	90	140	TO-3	**2N5038**	20	12	5	1	12	1200
20	160	125	120	TO-3	**BUX40**	8	15	4	1.2	10	1000
20	220	160	150	TO-3	**BUX11N**	10	15	4	0.6	8	800
20	250	200	150	TO-3	**BUX11**	10	12	4	0.6	6	600
20	300	250	150	TO-3	**BUX12**	10	10	4	1	5	500
25	120	80	175	TO-3	**BDY57**	20	10	4	1.4	10	1000
25	160	125	106	SOT-93	**BUX10P**	10	20	4	0.6	10	1000
25	160	125	150	TO-3	**BUX10**	10	20	4	0.6	10	1000
25	160	125	175	TO-3	**BDY58**	20	10	4	1.4	10	1000
25	160	140	106	SOT-93	**BU999**	12	25	2	0.8	10	1000
30	120	90	140	TO-3	**2N5671**	20	15	2	0.75	15	1200
30	150	120	140	TO-3	**2N5672**	20	15	2	0.75	15	1200
40	150	120	140	TO-3	**2N6033**	10	40	2	1	40	4000
40	250	200	250	TO-3	**BUV21**	10	25	4	0.6	12	1200
40	300	200	250	TO-3	**BUR21**	10	25	4	0.6	12	1200
40	300	250	250	TO-3	**BUV22**	10	20	4	1	10	1000
40	300	250	350	TO-3	**BUX22**	10	20	4	1	10	1000
40	350	250	250	TO-3	**BUR22**	10	20	4	1	10	1000
50	120	90	140	TO-3	**2N6032**	10	50	2.6	1.3	50	5000
50	160	125	250	TO-3	**BUV20**	10	50	4	0.6	25	2500
50	200	125	250	TO-3	**BUR20**	10	50	4	1	25	2000
60	300	200	350	TO-3	**BUR51**	15	50	4	1	30	2000
60	350	250	350	TO-3	**BUR52**	15	40	4	1.8	25	2000
70	200	125	350	TO-3	**BUR50**	15	50	4	1	35	2000
70	200	125	350	TO-3	**BUR50S**	15	50	4	1	35	2000

ALPHANUMERICAL INDEX DEVICE

LINEAR INTEGRATED CIRCUITS

LINEAR INTEGRATED CIRCUITS (continued)

DISCRETE POWER

SWITCHING REGULATOR MODULES

PACKAGES

HANDLING AND MOUNTING ICs IN PLASTIC POWER PACKAGES

Integrated circuits mounted in plastic power packages can be damaged, or reliability compromised, by inappropriate handling and mounting techniques. Avoiding these problems is simple if you follow the suggestions in this section.

Advances in power package design have made it possible to replace metal packages with more economical plastic packages in many high power applications. Most of SGS' power driver circuits, for example, are mounted in the innovative MULTIWATT® package, developed originally for high power audio amplifiers. Though the intrinsic reliability of these packages is now excellent the use of inappropriate techniques or unsuitable tools during mechanical handling can affect the long term reliability of the device, or even damage it. With a few simple precautions, careful designers and production engineers can eliminate these risks, saving both time and money.

BENDING AND CUTTING LEADS

The first danger area is bending and cutting the leads. In these processes it is important to avoid straining the package and particularly the area where the leads enter the encapsulating resin. If the package/lead interface is strained the resistance to humidity and thermal stress are compromised, affecting reliability.

There are five basic rules to bear in mind:

- Clamp the leads firmly between the package and the bend/cut point (figure 1).
- Bend the leads at least 3 mm from the package (figure 2a).
- Never bend the leads more than 90° and never bend more than once (figure 2b).
- Never bend the leads laterally (figure 2c).
- Make sure that the bending/cutting tool does not damage the leads.

Fig. 1 - Clamp the leads between the package and bend/cut point.

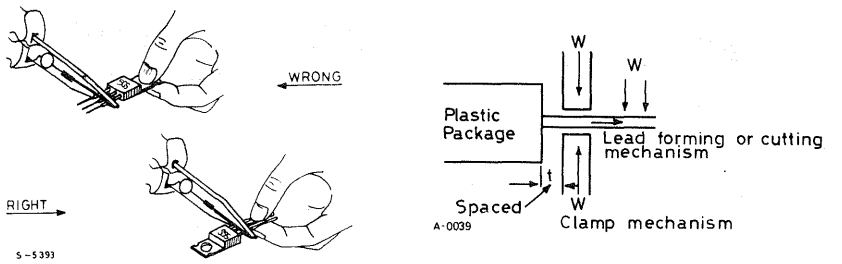
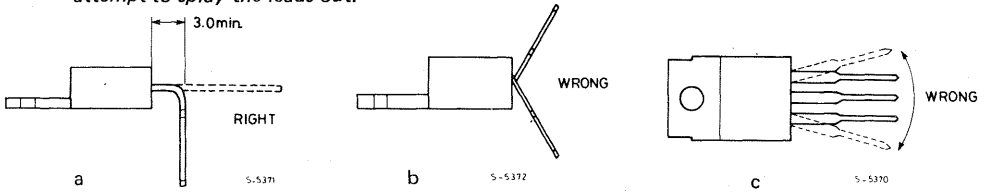


Fig. 2 - Bend the leads at least 3 mm. from the package, never bend leads more than 90° and never attempt to splay the leads out.



INSERTION

When mounting the IC on a printed circuit board the golden rule is, again, to avoid stress. In particular:

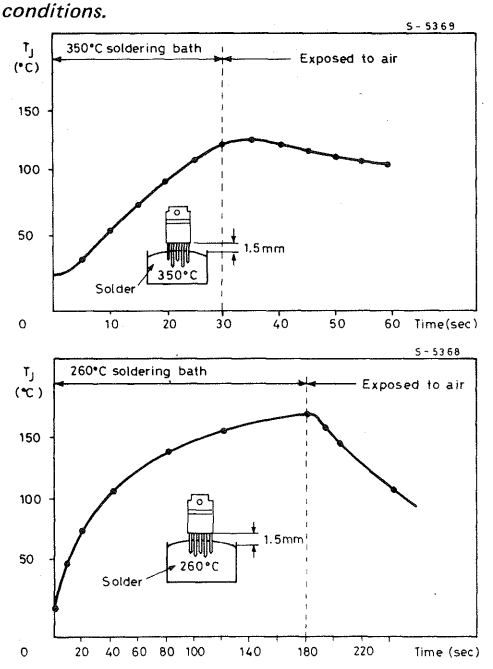
- Adhere to the specified pin spacing of the device; don't try to bend the leads to fit non-standard hole spacing.
- Leave a suitable space between the IC and the board. If necessary use a spacer.
- Take care to avoid straining the device after soldering. If a heatsink is used and it is mounted on the PC board it should be attached to the IC before soldering.

SOLDERING

The greater danger during soldering is overheating. If an IC is exposed to high temperature for an excessive period it may be damaged or reliability reduced.
Recommended soldering conditions are 260°C for ten seconds or 350°C for three seconds. Figure 3 shows the excess junction temperature of a PENTAWATT package for both methods.

It is also important to use suitable fluxes for the soldering baths to avoid deterioration of the leads or package resin. Residual flux between the leads or in contact with the resin must be removed to guarantee long term reliability. The solvent used to remove excess flux should be chosen with care. In particular, trichloroethylene ($CHCl : CCl_2$) – based solvents should be avoided because the residue can corrode the encapsulant resin.

Fig. 3 - The excess junction temperature of a PENTAWATT package in the suggested soldering conditions.

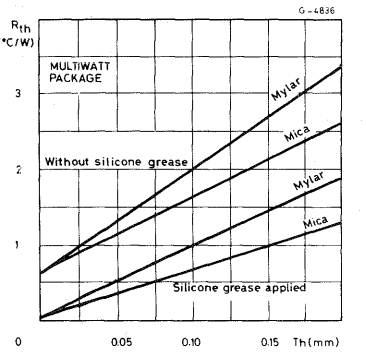


HEATSINK MOUNTING

To exploit the full capability of a power device a suitable heatsink must be used. The most important aspect from the point of view of reliability is that the heatsink is dimensioned to keep the junction temperature as low as possible. From a mechanical point of view, however, the heatsink must be designed so that it does not damage the IC. Care should also be taken in attaching the IC to the heatsink.

The contact thermal resistance between the device and the heatsink can be improved by adding a thin layer of silicon grease with sufficient fluidity to ensure uniform distribution. Figure 4 shows how the thermal resistance of a MULTIWATT package is improved by silicone grease.
An excessively thick layer or an excessively viscous silicon grease may have the opposite effect and could cause deformation of the tab.

Fig. 4 - The thermal resistance of a MULTIWATT package is improved by silicon grease. Here thermal resistance is plotted against grease thickness.



SGS plastic power packages – MULTIWATT, PENTAWATT and VERSAWATT – are attached to the heatsink with a single screw. A spring clip may also be used as shown in figure 5. The screw should be properly tightened to ensure that the package makes good contact with the heatsink. It should not be too tight or the tab may be deformed, breaking the die or separating the resin from the tab.

The appropriate tightening torque can be found by plotting thermal resistance against torque as shown in figure 6.
Suggested tightening torques for 3MA screws are 8 Kg/cm for VERSAWATT, PENTAWATT and MULTIWATT packages. If different screws, or sping clips, are used the force exerted by the tab must be equivalent to the force produced with these recommended torques.

Even if the screw is not overtightened the tab can be deformed, with disastrous results. If the surface of the heatsink is not sufficiently flat. The planarity of the contact surface between device and

Fig. 5 - MULTIWATT, PENTAWATT and VERSAWATT packages are attached to the heatsink with a single screw or a spring clip.

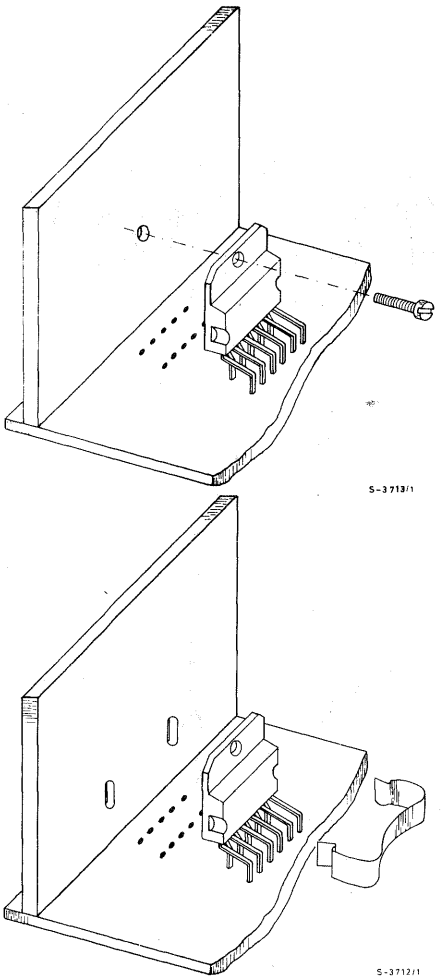
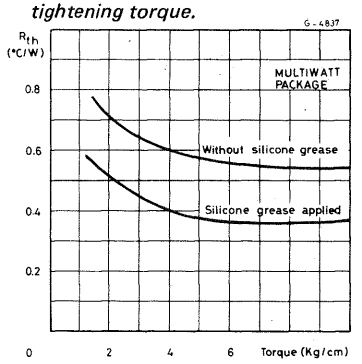
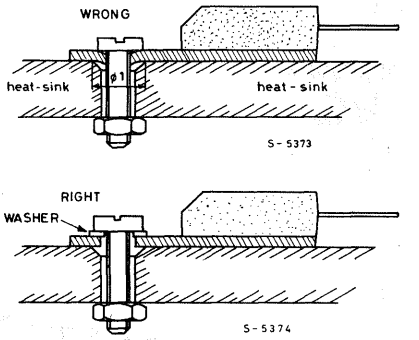


Fig. 6 - Contact thermal resistance depends on tightening torque.



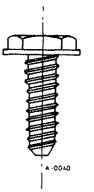
heatsink must be better than 50μm for PENTAWATT and VERSAWATT packages and less than 40μm for MULTIWATT packages.

Fig. 7 - The heatsink tab may be deformed if a washer or a wide-headed screw is not used.



Similar problems may arise if the screwhead is too narrow compared to the hole in the heatsink (figure 7).
The solution here is to use a washer to distribute the pressure over a wider area. An alternative is to use screws of the type shown in figure 8 which have a wide flat head. When self-tapping screws are used it is also important to provide an outlet for the material deformed as the thread is formed. Poor contact will result if this is not done. Another possible hazard arises when the hole in the heatsink is formed with a punch: a circular depression may be formed around the hole, leading to deformation of the tab. This may be cured by using a washer or by modifying the punch.

Fig. 8 - The recommended screw type looks like this.

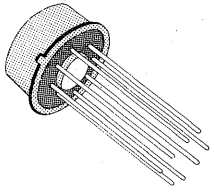


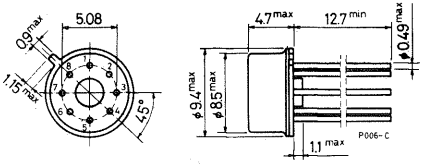
Serious reliability problems can be encountered if the heatsink and plrinted circuit board are not rigidly connected. Either the heatsink must be rigidly attached to the printed circuit board or both must be securely attached to the chassis. If this is not done the stresses and strains induced by vibration will be applied to the device and in particular to the lead/resin interface. This problem is more likely to arise when large boards and large heatsinks are used or whenever the equipment is subjected to heavy vibrations.

Packages

TO-99 (8 PIN)

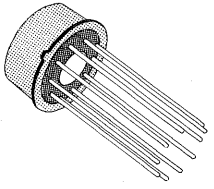
R_{th} = 155°C/W

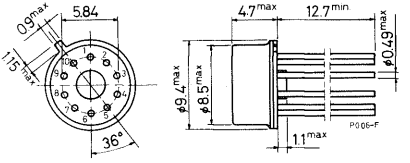




TO-100 (10 PIN)

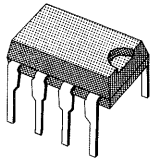
R_{th} = 155°C/W

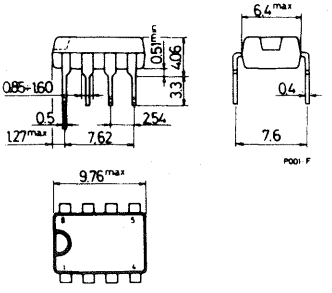




8-LEAD PLASTIC MINIDIP

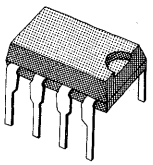
R_{th} = 120°C/W

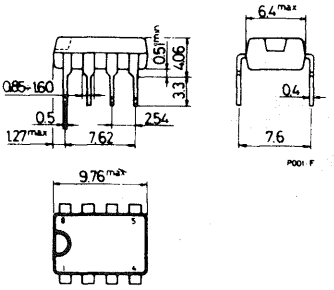


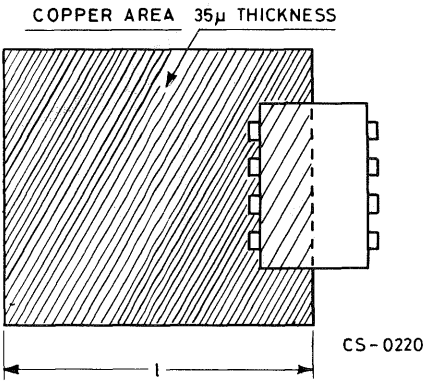


4 + 4 LEAD PLASTIC MINIDIP

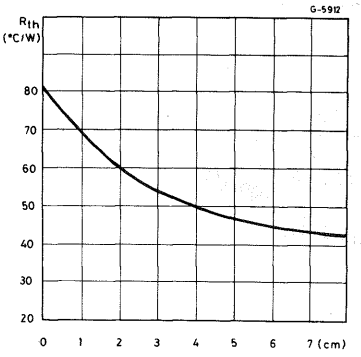
$R_{th\ j\text{-}pins} = 20°C/W$





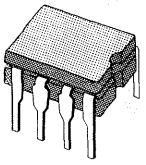


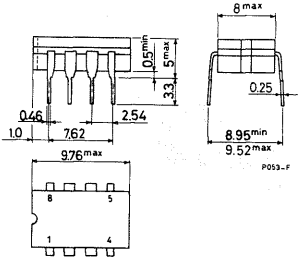
Thermal resistance of the PC offer vs. side "ℓ"



8-LEAD CERAMIC MINIDIP

$R_{th} = 150°C/W$

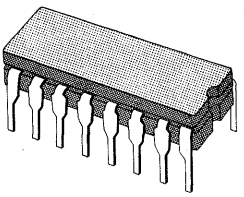


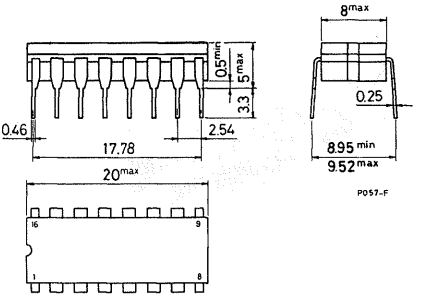


Pins 5 to 8 connected to substrate and used for heatsinking

Packages

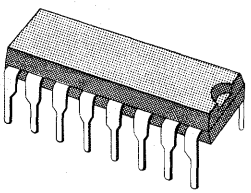
16-LEAD CERAMIC DIP

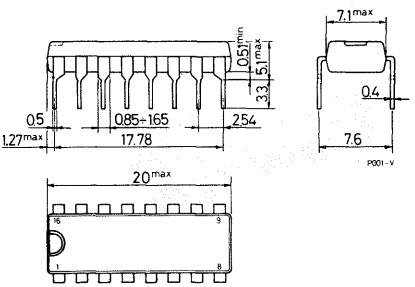




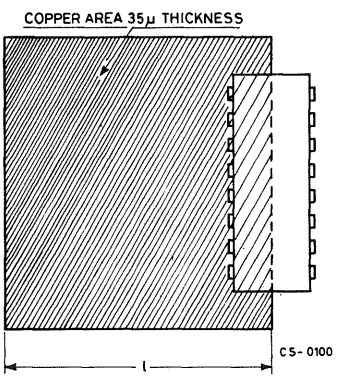
8 + 8 LEAD POWERDIP

$R_{th\ j\text{-}pins} = 15°C/W$
$R_{th\ j\text{-}amb} = 70°C/W$



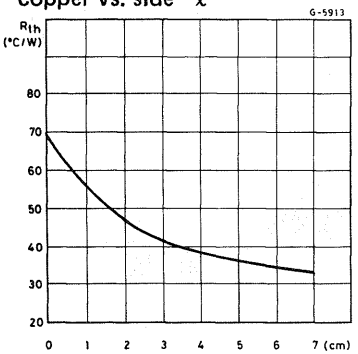


Pins 9 to 16-connected to substrate and used for heatsinking



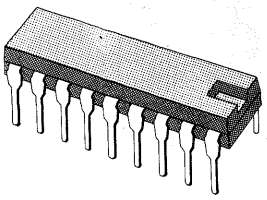
Using PC board copper as heatsink.

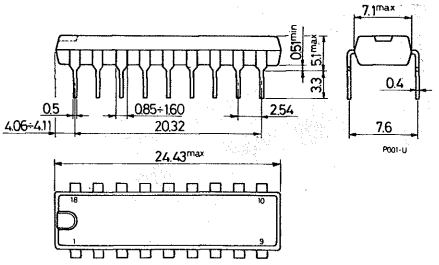
Thermal resistance of the PC copper vs. side "ℓ"



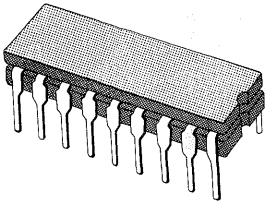
18-LEAD PLASTIC DIP

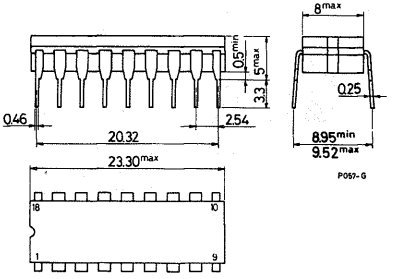
$R_{th} = 80°C/W$





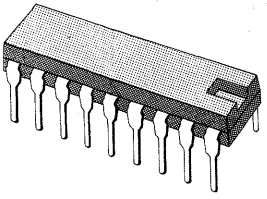
18-LEAD CERAMIC DIP

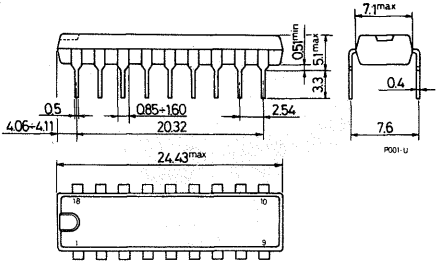




9 + 9 LEAD POWERDIP

$R_{th\ j\text{-}pins} = 15°C/W$
$R_{th\ j\text{-}amb} = 70°C/W$

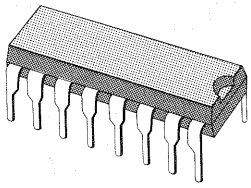


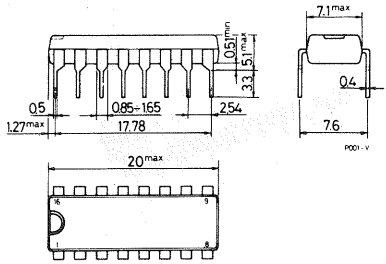


Packages

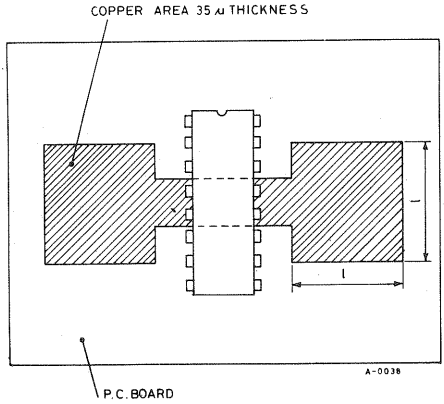
12 + 2 + 2 LEAD PLASTIC DIP

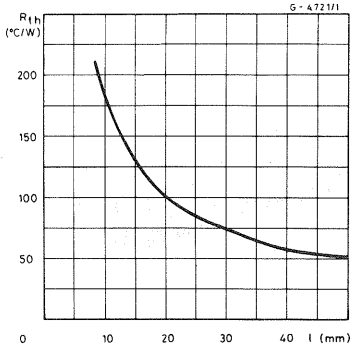
$R_{th\ j\text{-}pins} = 14°C/W$
$R_{th\ j\text{-}amb} = 80°C/W$





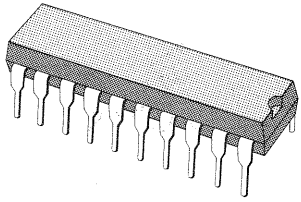
Four center pins connected to the substrate and used for heatsinking.

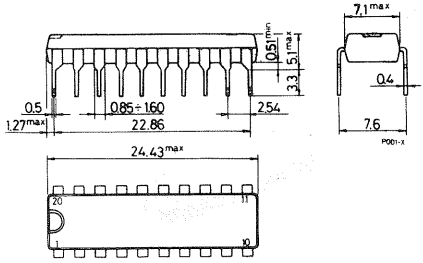




20-LEAD PLASTIC DIP

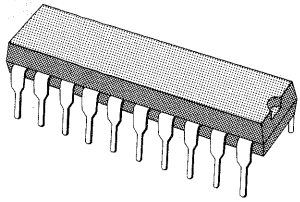
$R_{th\ j\text{-}amb} = 80°C/W$

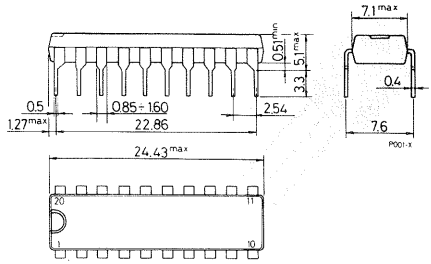


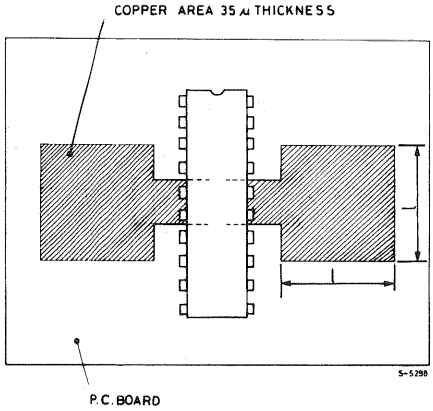


16 + 2 + 2 LEAD PLASTIC DIP

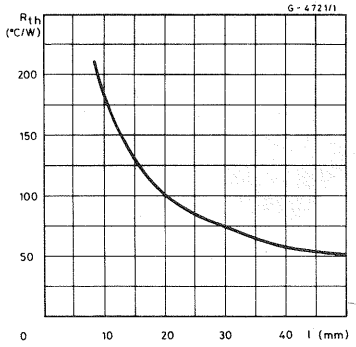
$R_{th\ j\text{-}pins} = 14°C/W$
$R_{th\ j\text{-}amb} = 80°C/W$





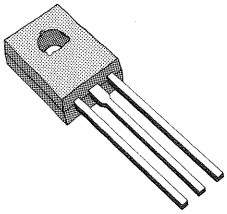


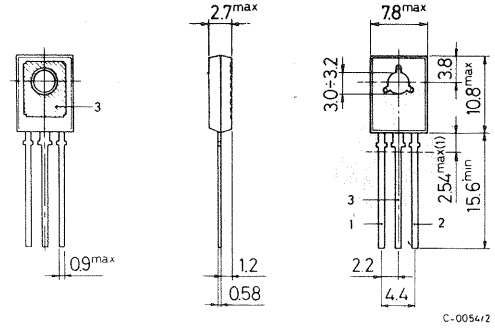
Thermal resistance of the PC copper vs. side "ℓ"



SOT-32

$R_{th} = 10°C/W$

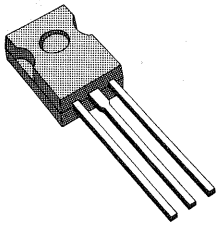


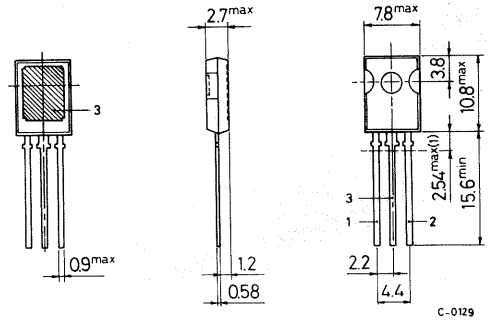


Packages

SOT-82

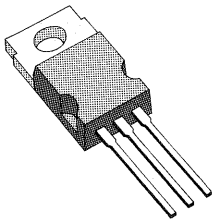
R_{th} = 8°C/W

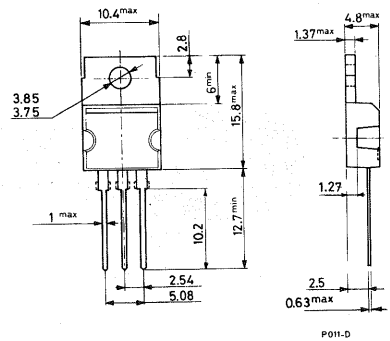




TO-220 (VERSAWATT)

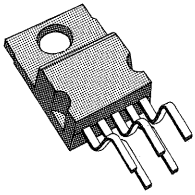
R_{th} = 3°C/W

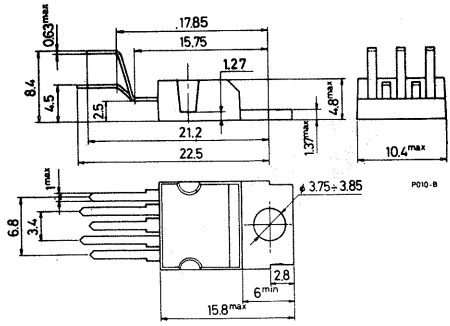




PENTAWATT®

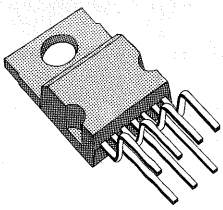
R_{th} = 3°C/W

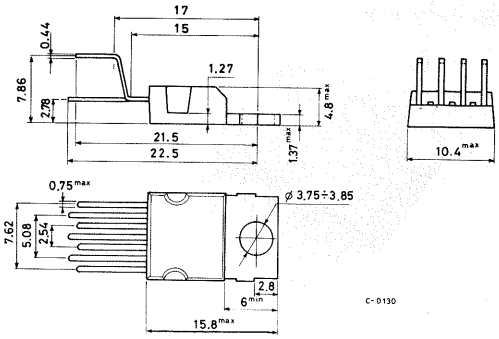




HEPTAWATT™

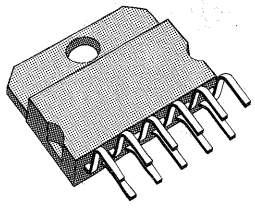
$R_{th} = 4°C/W$

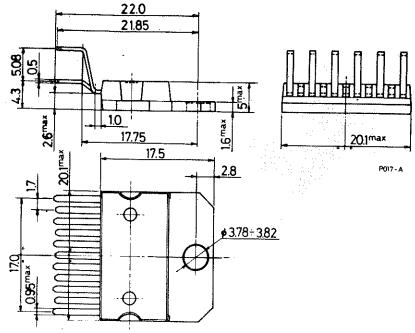




MULTIWATT - 11®

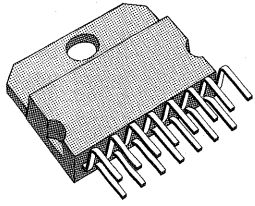
$R_{th} = 3°C/W$

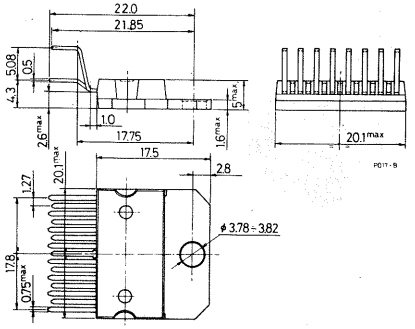




MULTIWATT - 15®

$R_{th} = 3°C/W$

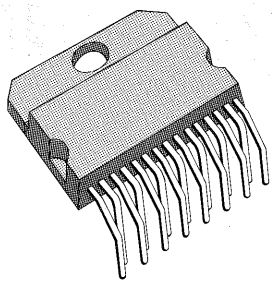


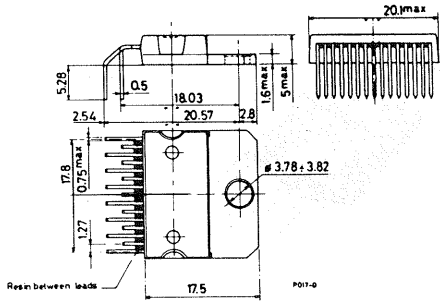


Packages

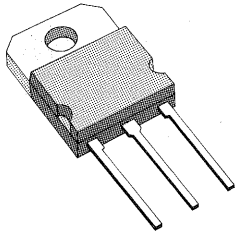
MULTIWATT 15 H

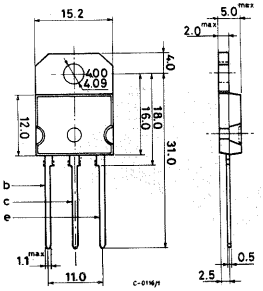
$R_{th} = 3°C/W$



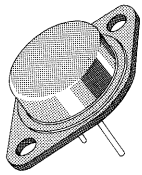


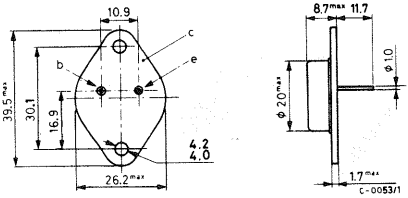
SOT-93



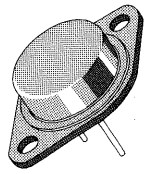


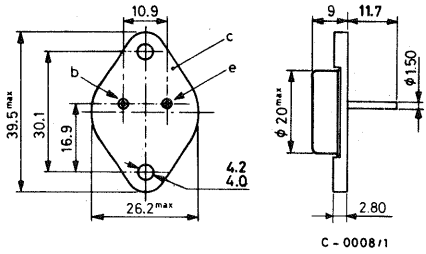
TO-3 (1)





TO-3 (2)





TO-3 (4 lead)

$R_{th} = 4°C/W$